# **ATT7022B** User Manual

Date: 2005-06-30

Rev: 1.04

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# Chapter 1 Introduction

## §1.1 Features

• High accuracy, less than 0.1% error over a dynamic range of 1000 to 1;
• Active energy measure accords with 0.2S, 0.5S, supports IEC 62053-22,GB/T 17883-1998
• Reactive energy measure accords with 2S, 3S, supports IEC 62053-23,GB/T 17882-1999;
• Provides fundamental wave, harmonic energy and total energy measure;
• Provides apparent energy measure;
• Supplies positive and negative active energy, reactive energy data;
• Supplies instantaneous active power, reactive power, and apparent power data;
• Supplies power factor, phase difference, line frequency data;
• Supplies voltage RMS, current RMS data; RMS precision overmatches 0.5%;
• Provides voltage and current phase sequence detecting;
• Provides RMS output for 3-phase current vector summation;
• Provides RMS output for 3-phase voltage vector summation;
• Provides voltage middle angle measure;
• Provides voltage-lost detecting;
• Provides indication for negative power;
• Provides calibration pulse output for active, reactive and apparent energy;
• Provides calibration pulse output for fundamental wave active and reactive energy;
• Selectable calculating mode for 3 phase energy combined;
• Built-in temperature sensor;
• Adjustable meter constant;
• Adjustable startup current;
• Accurate measure for active, reactive and apparent power which contain 21st harmonic;
• Provides gain and phase compensation, nonlinear compensation for little current;
• Easy to use SPI port to communicate with host MCU;
• Compatible with 3-phase 3-wire and 3-phase 4-wire services;
• Single +5V power supply;
• QFP44 package.

## §1.2 Functional description

ATT7022B is a high accuracy 3-phase electronic energy metering chip which is suitable for 3-phase 3-wire and 3-phase 4-wire services.

ATT7022B incorporates 7 second-order sigma-delta ADCs, reference circuitry and all the signal processing required calculating power, energy, RMS data, power factor and frequency.

ATT7022B is suitable for measuring active power, reactive power, apparent power, active energy, and reactive energy for each phase and 3 phases combined; it is also suitable for measuring voltage RMS, current RMS, power factor, phase difference, and frequency. ATT7022B is qualified for 3-phase multifunctional electronic energy meter.

ATT7022B supports software calibration for gain, phase. Two pulses for active and reactive power (CF1, CF2) can be used directly to calibrate error. Refer to chapter 3 for detailed calibration method.

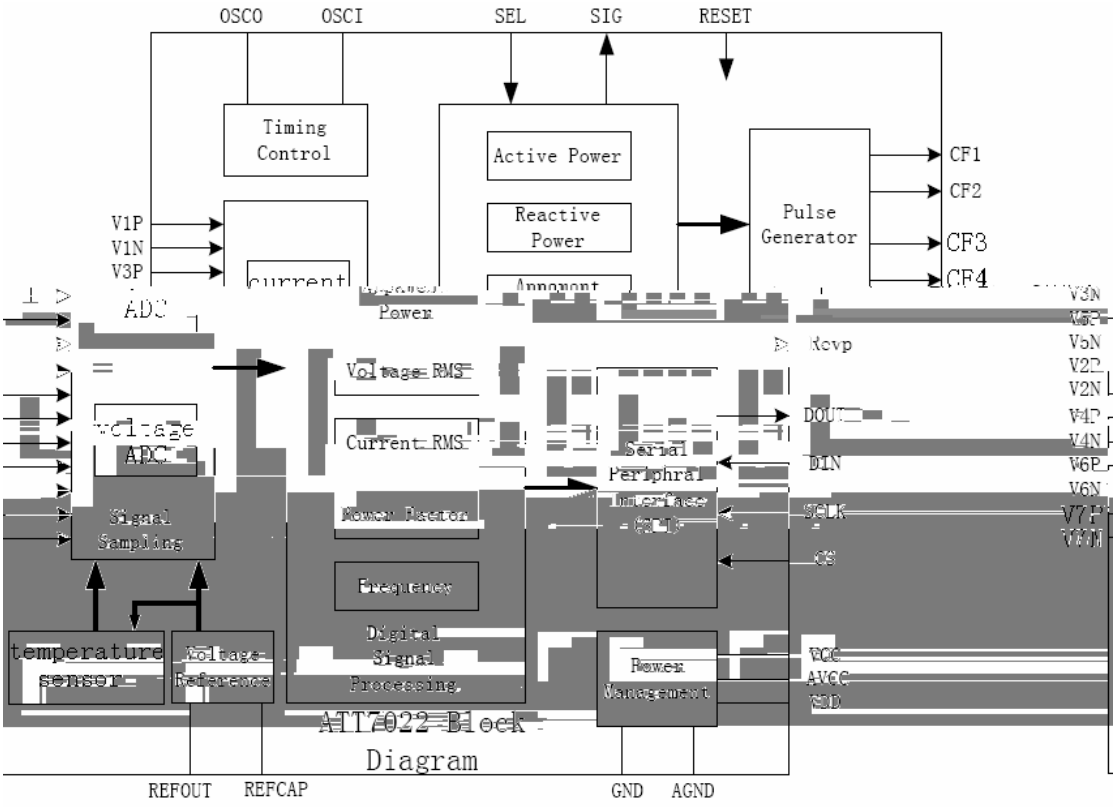
ATT7022B supports fundamental wave active power and reactive power measurement. The two pulses output (CF3, CF4) can be used to calibrate fundamental wave power error.

ATT7022B provides two kinds of apparent energy output: RMS apparent energy and PQS apparent energy, CF3 and CF4 could also be used as apparent energy pulse output.

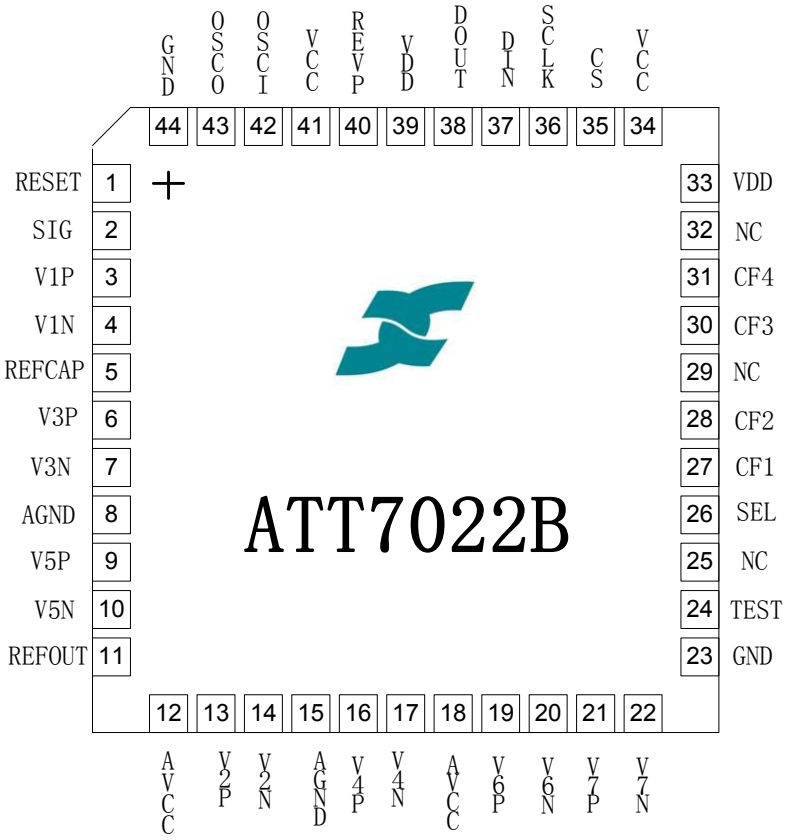
SPI port is used to transfer data to and from host MCU for all measuring result and calibration data. Refer to chapter 4 for detailed SPI reading and writing method.

Power supply monitor circuitry safeguards ATT7022B's performance.

## §1.3 Block diagram



## §1.4 Pin definition




| Pin | Name | I/O | Description |
|---|---|---|---|
| 1 | RESET | I | ATT7022B reset, low active with internally pull-up 47K resistance. |
| 2 | SIG | O | SIG would go low when ATT7022B power on reset or unconventional reset. After the host MCU sends calibration data via SPI, SIG would goes high immediately. |
| 3,4 | V1P/V1N | I | Fully differential mode analog inputs for phase A current channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry. An over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 5 | REFCAP | O | Internal reference voltage, 2.4V, can be connected to external reference voltage. This pin should be decoupled with a 10μF and a 0.1uF capacitor to AGND. |
| 6,7 | V3P/V3N | I | Fully differential mode analog inputs for phase B current channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry. An over voltage of ±6V can be sustained on these inputs without risk of |

| | | | |
|---|---|---|---|
| | | | permanent damage. |
| 8,15 | AGND | AGND | The analog ground is the ground reference for all analog circuitry. |
| 9,10 | V5P/V5N | I | Fully differential mode analog inputs for phase C current channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry. An over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 11 | REFOUT | O | Reference voltage output, acts as bias for input signals**.** |
| 12,18 | AVCC | AVCC | Analog power supply, the supply voltage should be maintained at 5V±5％ for specified operation. This pin should be decoupled with a 10μF and a 0.1uF capacitor to AGND. |
| 13,14 | V2P/V2N | I | Fully differential mode analog inputs for phase A voltage channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry. An over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 16,17 | V4P/V4N | I | Fully differential mode analog inputs for phase B voltage channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry. An over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 19,20 | V6P/V6N | I | Fully differential mode analog inputs for phase C voltage channel. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry. An over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 21,22 | V7P/V7N | I | Fully differential mode analog inputs for NO.7 ADC. The maximum input signal level is ±1.5V. Both inputs have internal ESD protection circuitry and in addition an over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 23,44 | GND | GND | Digital ground. |
| 24 | TEST | I | Test pin, should tie to GND normally. Internally pull-down 47K resistance. |
| 25,29,32 | NC | --- | No connection. |
| 26 | SEL | I | System mode selection, high for 3-phase 4-wire, |

| | | | |
|---|---|---|---|
| | | | low for 3-phase 3-wire. Internally pull-up 300K resistance. |
| 27 | CF1 | O | Active energy pulse output. This output can be used for operational and calibration purposes. The frequency of CF1 stands for 3 phases combined average active power. |
| 28 | CF2 | O | Reactive energy pulse output. This output can be used for operational and calibration purposes. The frequency of CF2 stands for 3 phases combined average reactive power |
| 30 | CF3 | O | CF3: fundamental wave active energy pulse output. The frequency of CF3 stands for 3 phase combined average active power of fundamental wave.<br>CF3 can also be configured as apparent energy pulse output (RMS). |
| 31 | CF4 | O | CF4: fundamental wave reactive energy pulse output The frequency of CF4 stands for 3 phase combined average reactive energy of fundamental wave.<br>CF4 can also be configured as apparent energy pulse output (PQS). |
| 33,39 | VDD | VDD | 3.0V Power output. This pin should be decoupled with a 10μF and a 0.1uF capacitor to GND. |
| 34,41 | VCC | VCC | Digital power supply, the supply voltage should be maintained at 5V±5%. This pin should be decoupled with a 10μF and a 0.1uF capacitor to GND. |
| 35 | CS | I | SPI selection signal, low active, Internally pull-up 200K resistance. |
| 36 | SCLK | I | SPI serial clock input (Schmitt).<br>Note: Data is output at the rising edge and input at the falling edge. |
| 37 | DIN | I | SPI serial data input (Schmitt). Internally pull-down 200K resistance. |
| 38 | DOUT | O | SPI serial data output. It is high-impedance output when CS is high. |
| 40 | REVP | O | Goes high when any phase's active power is negative, goes low when all 3 phases' active power is positive. |
| 42 | OSCI | I | System oscillator input.<br>Oscillator frequency is 24.576MHz. |
| 43 | OSCO | O | System oscillator output. |

## §1.5 Application diagram

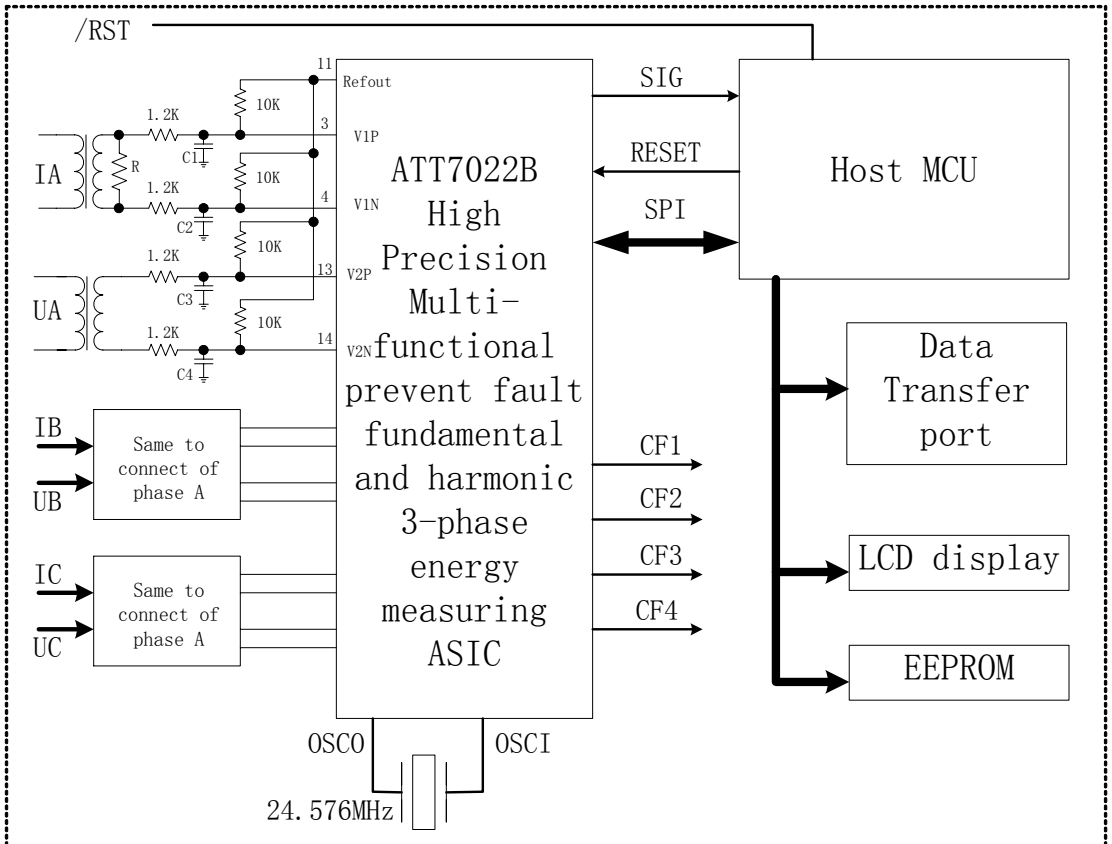



Diagram 1-5-1 ATT7022B typical application diagram

# Chapter 2 System Functions

## §2.1 Power supply monitor

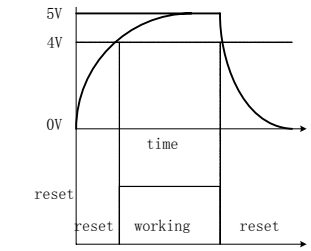


Diagram 2-1-1 power supply monitor

ATT7022B contains an on-chip power supply monitor. The analog supply (AVCC) is continuously monitored by the ATT7022B. If the supply is less than 4V±5%, the ATT7022B will be reset. This is useful to ensure correct device start-up and operation at power-on and power-down. The power supply monitor has built in delay and filtering circuits. This gives a high degree of immunity to false trigger due to noisy supplies, as illustrated in the figure 2-1. The power supply should be decoupled so that the ripple at AVCC does not exceed 5V±5% for normal operation.

## §2.2 System reset

ATT7022B provides two kinds of reset method: hardware reset and software reset.

Hardware reset is executed via external RESET pin, which has internal 47K pull-up resistance. So in normal working, the RESET pin is set to logic high; If RESET pin is pulled to low level overstep 20us, ATT7022B would be reset; and when RESET pin goes to logic high, ATT7022B would go to normal working state from reset state.

Software reset is executed via SPI port; if we write 0xD3 to SPI port, ATT7022B would be reset and start working renewedly from initial state.

The SIG pin is set to logic high in reset state. After ATT7022B goes to normal working state from reset state, SIG pin would be pulled to low level from high level in about 500us, then the chip will start normal working and the calibration data could be written in. Once the calibration data is written, SIG pin would go to high level immediately.

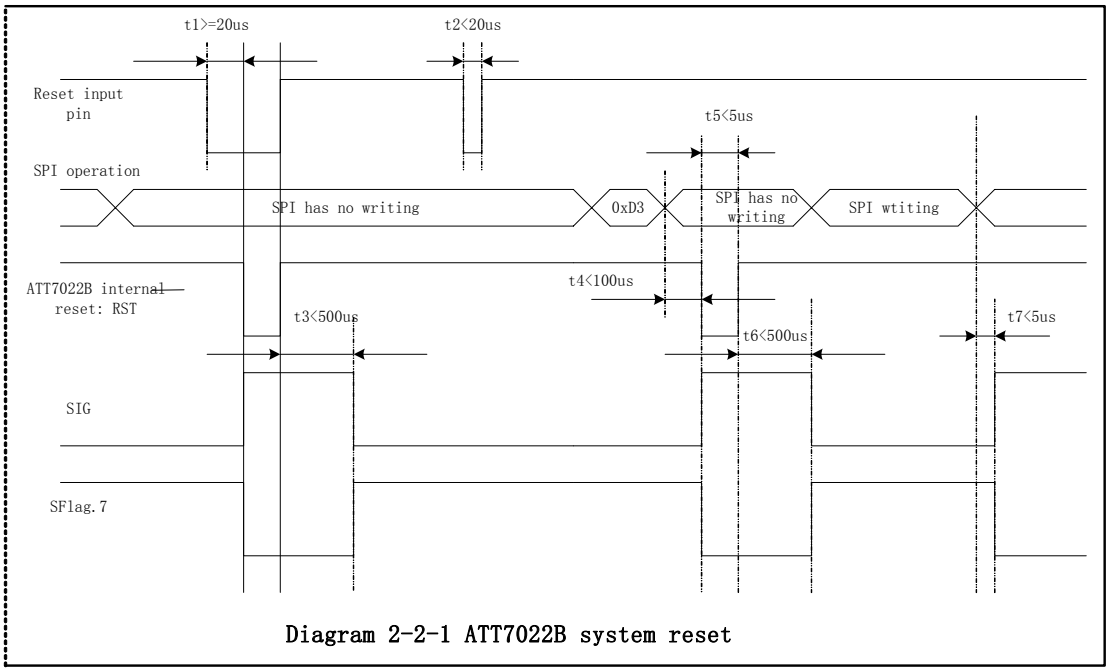


Diagram 2-2-1 ATT7022B system reset

## §2.3 ADC

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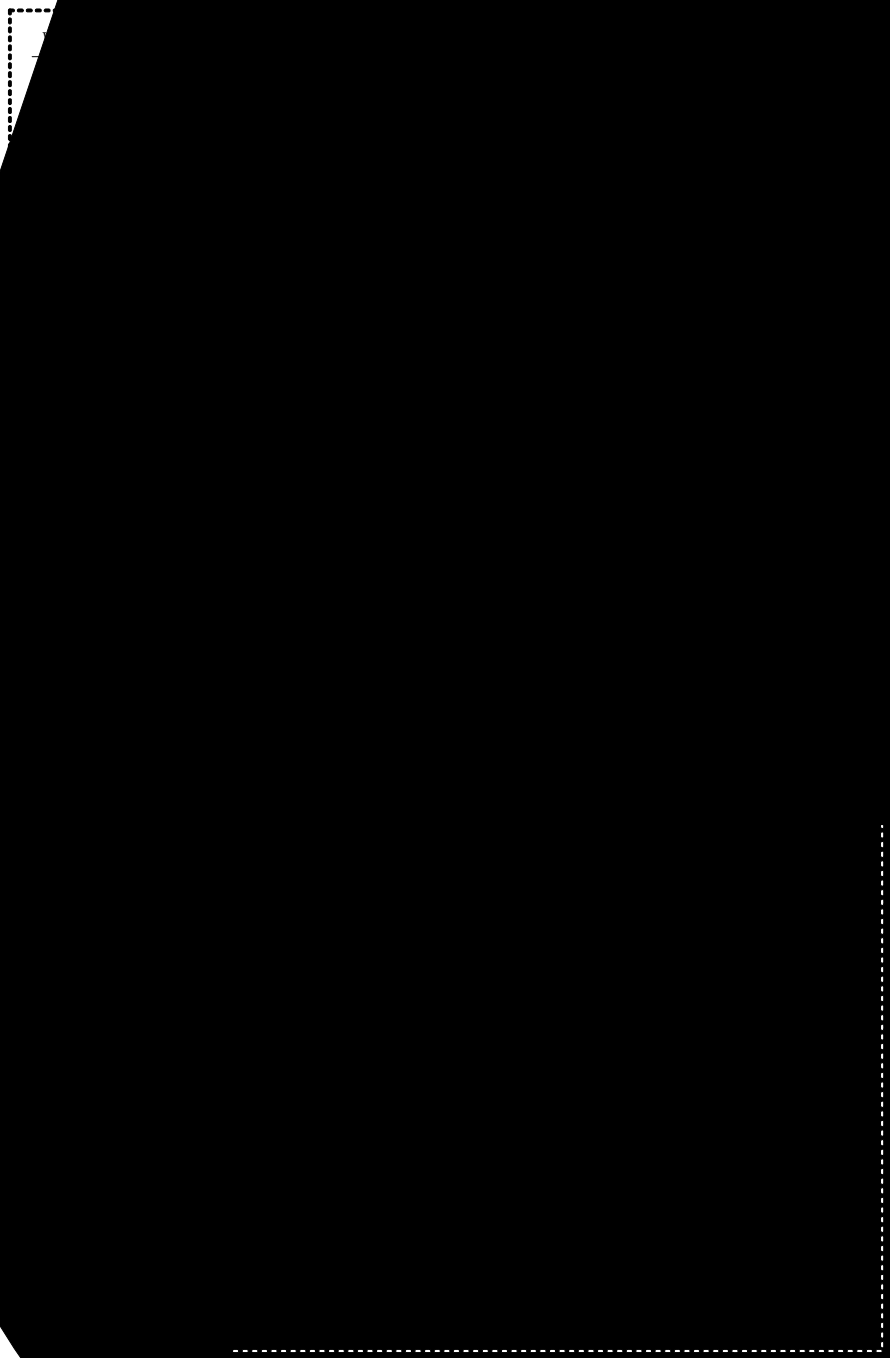


## §2.4 Active power measure

Calculation of active power for each phase is achieved by a series of multiplication, addition and digital filtering, which act on input voltage and current signals after removing dc offset.

The over-sampling of sigma-delta ADC guarantees sampling rate of input signals, and the sampled data contains information for up to 21st harmonic. And according to the formula P= $\frac{1}{N}\sum_{n=0}^{N}U(n)\bullet I(n)$, the active power contains information for up to 21st harmonic.

The measure elements of active power is illustrated in the nether figure, 3-phase combined active power Pt=Pa+Pb+Pc.

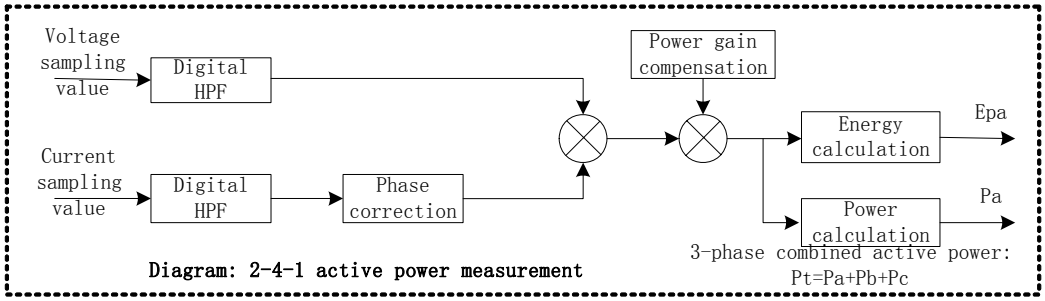



Diagram: 2-4-1 active power measurement

## §2.5 Active energy measure

Calculation of active energy is achieved via instantaneous active power integrating to the time.

The formula of single phase active energy: $Ep = \int p(t)dt$

The 3-phase combined active energy could be summated according to algebraic addition mode or absolute addition mode, which could be set through registers.

Algebraic addition mode: Ept=Epa+Epb+Epc

Absolute addition mode: Ept=|Epa|+|Epb|+|Epc|

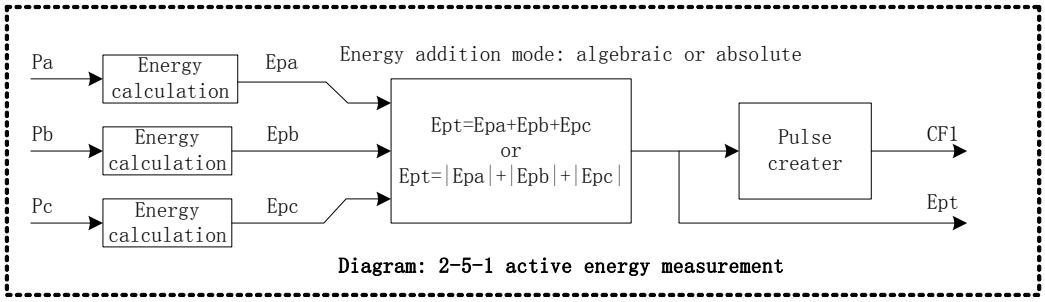



Diagram: 2-5-1 active energy measurement

## §2.6 Reactive power measure

According to real reactive power (sine reactive power) well-defined formula, the reactive power $Q = \sum_{n=1}^{\infty} U_n I_n \sin(\varphi)$.

Calculation of reactive power is similar to the calculation of active power. The only difference is that the voltage signals are 90 degree phase shifted. The metrical bandwidth is restricted by the bandwidth of digital phase-shifted filter. The metrical bandwidth of ATT7022B reactive power could be also up to 21st harmonic.

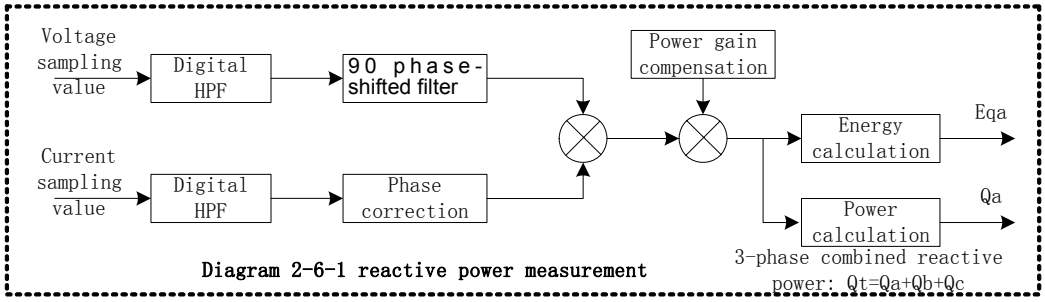



Diagram 2-6-1 reactive power measurement

The digital 90˚ phase-shifted filter in ATT7022B has ascendant frequency response characteristic, as illustrated in the figure 2-6-2. It is a linear filter with the amplitude-frequency characteristic of 1; and all frequency components in the frequency-band would be processed -90° phase-shifted. So ATT7022B can achieve corking measurement veracity even when measuring high-order harmonic reactive power.

Note: when calibrating reactive power, we must insure that the reactive power arithmetic of standard-meter is same to ATT7022B reactive power arithmetic; otherwise the difference of arithmetic would bring definite error, especially to harmonic reactive power.

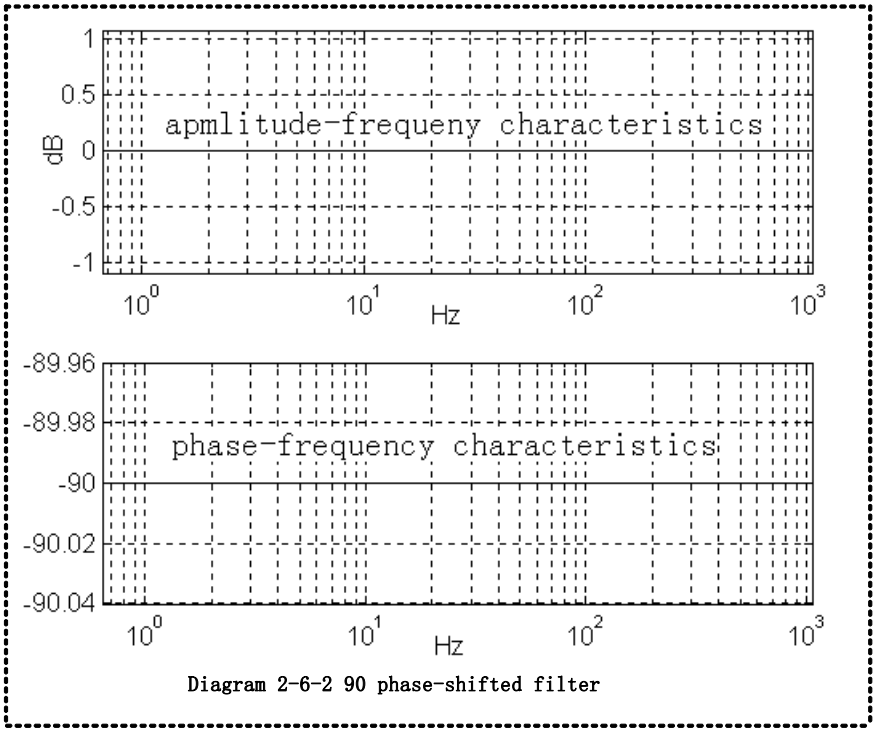



Diagram 2-6-2 90 phase-shifted filter

## §2.7 Reactive energy measure

Calculation of reactive energy is achieved via instantaneous reactive power integrating to the time.

The formula of single phase reactive energy: $Eq = \int q(t)dt$

The 3-phase combined reactive energy could be summated according to algebraic addition mode or absolute addition mode, which could be set through registers.

Algebraic addition mode: Eqt=Eqa+Eqb+Eqc

Absolute addition mode: Eqt=|Eqa|+|Eqb|+|Eqc|

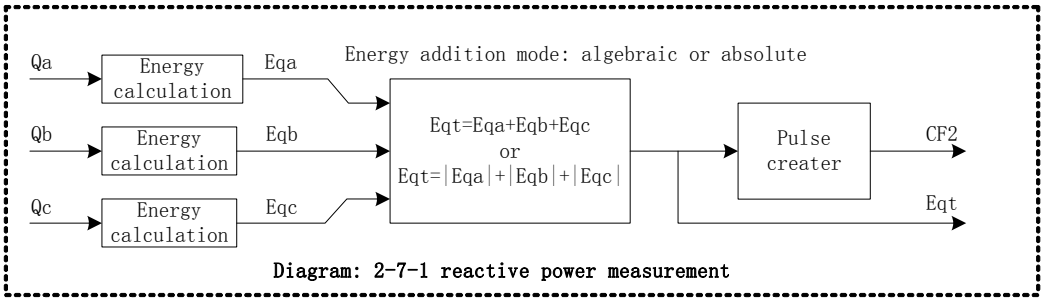



Diagram: 2-7-1 reactive power measurement

## §2.8 apparent power measure

Apparent power has two kinds of calculation formula:

PQS apparent power formula 1: $S = \sqrt{P^2 + Q^2}$

RMS apparent power formula 2: S=Urms*Irms

Because of ATT7022B could supply voltage RMS and current RMS directly, RMS apparent power as described in formula 2 can be achieved convenient via external MCU, so ATT7022B supplies only the apparent power value which is achieved by PQS apparent power formula 1, as illustrated in the nether figure.

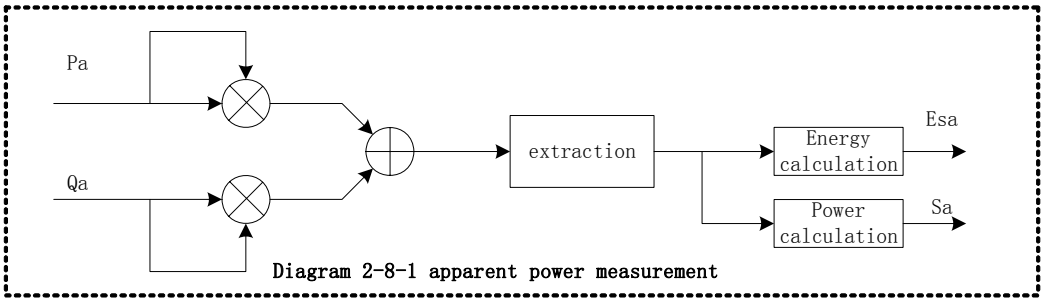



Diagram 2-8-1 apparent power measurement

ATT7022B calculates 3-phase combined apparent power according to formula 1, which bases on 3-phase combined active power and 3-phase combined reactive power, as illustrated in the nether figure.

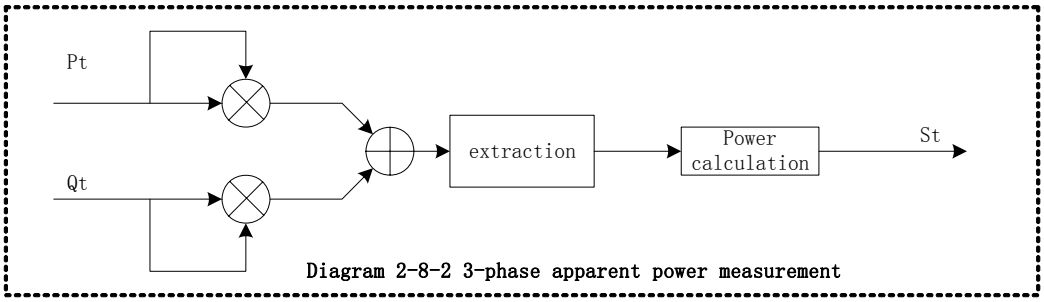



Diagram 2-8-2 3-phase apparent power measurement

## §2.9 apparent energy measure

Apparent energy is defined as apparent power integrating to the time. Because of apparent power have two kinds of calculation formula, so ATT7022B supplies two kinds of apparent energy.

The PQS apparent energy is calculated according to formula 1, as illustrated in the nether figure. The 3-phase combined PQS apparent energy pulse is output via CF4.

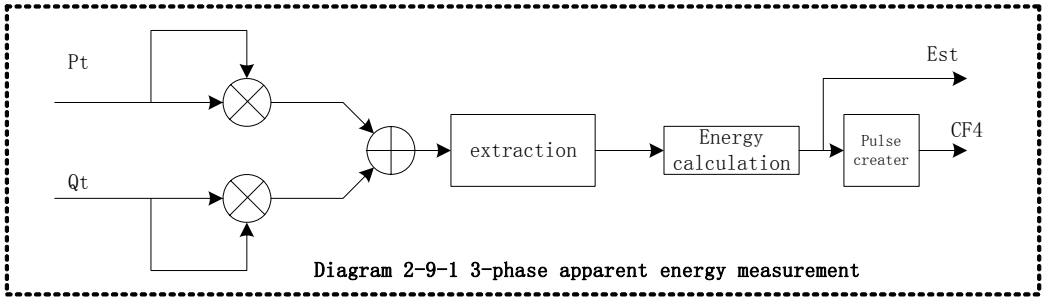



Diagram 2-9-1 3-phase apparent energy measurement

The RMS apparent energy is calculated according to formula 2, as illustrated in the nether figure. The 3-phase combined RMS apparent energy pulse is output via CF3.

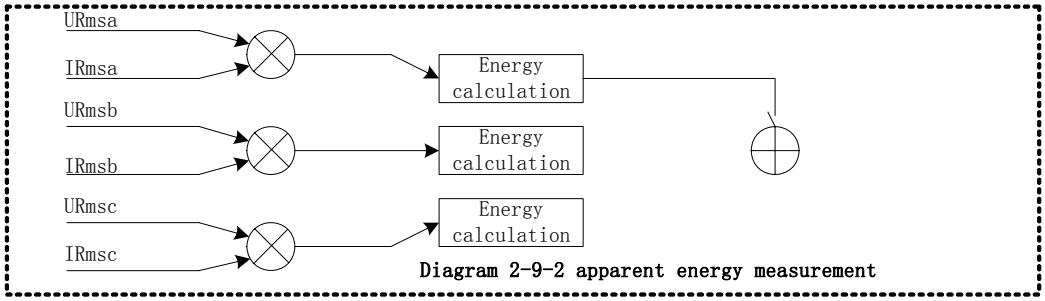



Diagram 2-9-2 apparent energy measurement

single phase voltage in A/B/C 3 phase as benchmark of line-frequency measure. Measurable line-frequency range is 10Hz ~ 500Hz.

## §2.13 Power factor measure

Power factor calculation formula: $Pf=sign(Q)\times\frac{abs(P)}{abs(S)}$

The sign of power factor is determined by the sign of reactive power.

## §2.14 Voltage and current phase angle measure

According to electrotechnician theory, power factor Pf=cos(Pg), thereinto Pg is middle angle of voltage and current. In ATT7022B, the voltage and current phase angle is defined as: Pg= sign(Q)*acos(|Pf|). According to this method, ATT7022B could supply 3-phase combined power factor to 3-phase combined phase angle reference: Pgt= sign(Q)*acos(|Pft|)

ATT7022B phase angle Pg could only be denoted as ±90°, the sign is same as power factor. If we want to use 0°～360° denoted different quadrant phase angle, we need to do some switchover as follows:

If active power is positive, reactive power is also positive, actual phase angle is Pg;

If active power is positive, reactive power is negative, actual phase angle is 360°+Pg;

If active power is negative, actual phase angle is 180°-Pg.

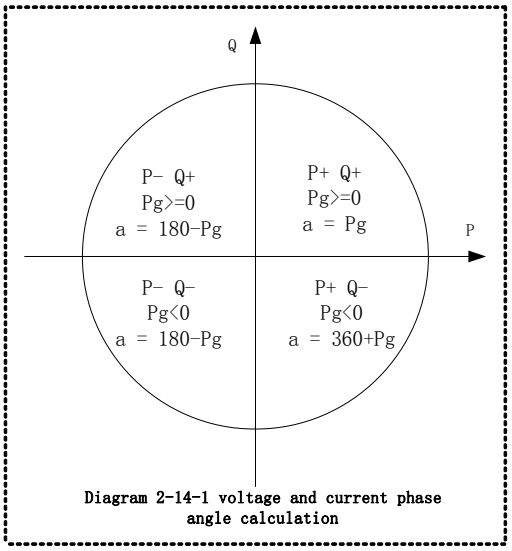



Diagram 2-14-1 voltage and current phase angle calculation

## §2.15 Voltage middle angle measure

The precision of ATT7022B voltage middle angle measure is about 5°. There are 3 registers in ATT7022B: YUaUb, YUaUc, YUbUc, which denote middle angle of AB/AC/BC phase voltage. The data will update every 1/3 second.

Note: Voltage middle angle measure function need to be turned on via voltage middle angle measure enable control register EnUAngle. It is recommended that we should open this function only when we need to output the angle values, otherwise we should close this function.

## §2.16 Voltage phase sequence measure

ATT7022B can detect voltage phase sequence, but the voltage phase sequence detection criterion of 3-phase 3-wire and 3-phase 4-wire is not same.

In 3-phase 4-wire mode, voltage phase sequence detection detects according as the zero crossing point sequence of A/B/C 3 phase voltage. The correct criterion of voltage phase sequence is phase A voltage cross zero －> phase B voltage cross zero －> phase C voltage cross zero, or else voltage phase sequence is wrong. In addition, if any phase of A/B/C has no voltage signal input, ATT7022B would also regard voltage phase

sequence as wrong.

In 3-phase 3-wire mode, voltage phase sequence detection detects according as the middle angle of phase A voltage and phase C voltage. If the middle angle of phase A voltage and phase C voltage is about 300°, ATT7022B would regard voltage phase sequence as right, or else voltage phase sequence is wrong.

The flag of voltage phase sequence is in flag register SFlag. SFlag[bit3] = 1 denotes A/B/C voltage phase sequence is wrong, SFlag[bit3] = 0 denotes A/B/C voltage phase sequence is wrong.

## §2.17 Current phase sequence measure

ATT7022B can detect current phase sequence. Current phase sequence detection detects according as the zero crossing point sequence of A/B/C 3 phase current. The correct criterion of current phase sequence is phase A current cross zero －> phase B current cross zero －> phase C current cross zero, or else current phase sequence is wrong. In addition, if any phase of A/B/C has no current signal input, ATT7022B would also regard current phase sequence as wrong.

The flag of current phase sequence is in flag register SFlag, SFlag[bit4] = 1 denotes A/B/C current phase sequence is wrong, SFlag[bit4] = 0 denotes A/B/C current phase sequence is right

Note: current phase sequence detection function need to be turned on via phase detection enable control register EnDtlorder. We should close this function except when we need use it.

## §2.18 Start-up and creep setting

ATT7022B implements start-up and creep via judging the value of current and start-up threshold. If ATT7022B detected any one phase current was higher than start-up threshold, the corresponding phase would start measure. If ATT7022B detected any one phase current was lower than start-up threshold, the corresponding phase would stop measure.

After power on reset, the default value of ATT7022B start-up current threshold register ‘Istartup’ is 0x000280, which denotes ATT7022B start-up at 0.1% and creep at 0.08% when input sampling signal is 100mv in rated current Ib.

## §2.19 Power direction judgement

ATT7022B supplies real time power direction judgement, which could implentment four-quadrant power measurement expediently.

Negative power indication REVP: if any one phase active power is negative, REVP would output logic high; REVP goes low when all 3 phase power is positive.

Power direction indication register PFlag: used to indicate the direction of A/B/C 3-phase combined active and reactive power.

Bit0-3: indicate the direction of A, B, C, and 3-phase combined active power respectively, 0 denotes positive, 1 denotes negative.

Bit4-7: indicate the direction of A, B, C, and 3-phase combined reactive power respectively, 0 denotes positive, 1 denotes negative.

## §2.20 Loss of voltage detecting

ATT7022B can detect A/B/C 3 phase voltage loss status based on configured threshold voltage.

Threshold voltage could be configured via voltage loss threshold setting register FailVoltage. After power on reset, the voltage loss threshold is set to different values based on current working mode (3-phase 3-wire/3-phase 4-wire), If voltage RMS has not being calibrated, in 3-phase 4-wire mode, threshold is about 50mv in voltage channel; in 3-phase 3-wire mode, threshold is about 300mv in voltage channel. If voltage RMS has being calibrated, voltage loss threshold setting register FailVoltage must be configured renewedly, please refer to the section 3.3.9, “voltage loss threshold setting”.

Loss of voltage status is indicated by status flat register: SFlag.

SFlag bit0/1/2 = 1 denotes A/B/C 3-phase voltage is lower than configured threshold voltage, SFlag bit0/1/2 = 1 denotes A/B/C 3-phase voltage is higher than configured threshold voltage.

## §2.21 Hardware port detecting

ATT7022B can detect hardware port automatically. System will reset when hardware port changes.

The external hardware input port used by ATT7022B is SEL.

## §2.22 On chip temperature detecting

ATT7022B has a built-in temperature sensor, while ATT7022B supplies a 8–bit ADC sampling output temperature data. The differentiate rate of temperature data is 1℃.

## §2.23 Fundamental wave and harmonic measure function

ATT7022B supplies fundamental wave and harmonic energy measurement. ATT7022B can separate fundamental wave component and harmonic component in voltage and current signal, provides accurate measurement to fundamental wave power, fundamental wave energy, harmonic power and harmonic energy.

Introduction of fundamental wave meter:

ATT7022B selects fundamental wave meter mode when fundamental wave measurement enable control register EnLineFreq = 0x007812, fundamental wave measurement and harmonic measurement switch select register EnHarmonic ≠ 0x0055AA. In the fundamental wave meter mode, the port CF3 output fundamental wave active pulse and the port CF4 output fundamental wave reactive pulse.

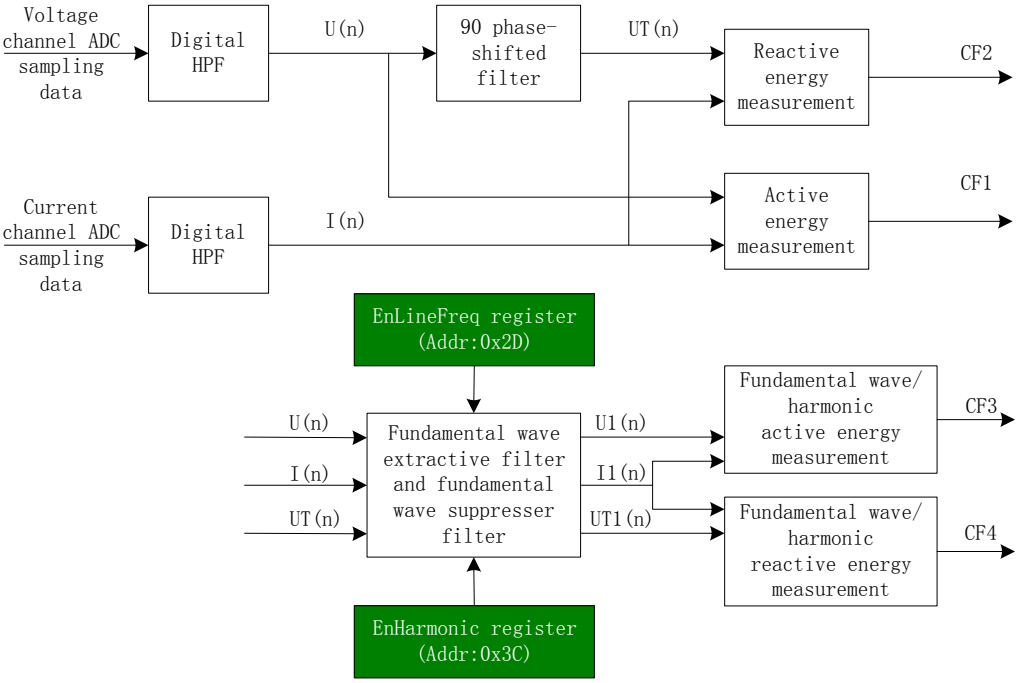



Diagram 2-23-1 fundamental wave/harmonic energy measurement

Fundamental wave extractive filter and fundamental wave suppresser complete fundamental wave or harmonic measurement function. The fundamental wave extractive filter can attenuate harmonic signals higher than 3st (150Hz), pass the fundamental wave component to be measured and the harmonic attenuation rate is up to -30dB. The fundamental wave suppresser attenuate fundamental wave signal, pass the harmonic component to be measured and the fundamental wave attenuation rate is up to -30dB.

Fundamental wave active power, fundamental wave reactive power, fundamental wave apparent power, fundamental wave phase angle, fundamental wave power factor, and fundamental wave voltage could be selected via fundamental wave voltage power output select register SelectPQSU. If SelectPQSU = 0x001228, the corresponding power, voltage, phase, phase angle registers would output fundamental wave data. If SelectPQSU ≠ 0x001228, the corresponding power, voltage, phase, phase angle registers would hold primary function unchanged.

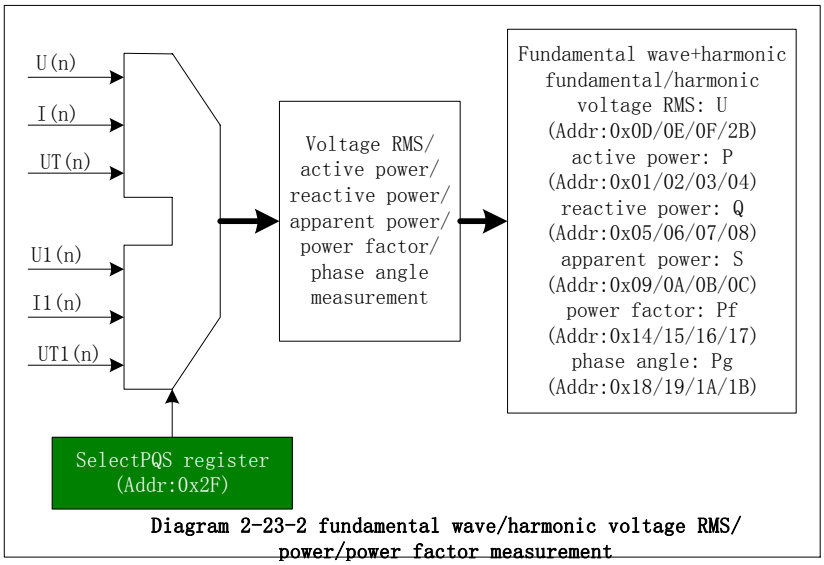



**Diagram 2-23-2 fundamental wave/harmonic voltage RMS/ power/power factor measurement**

Fundamental wave power can be calibrated via fundamental wave power calibration register. Please refer to fundamental wave calibration section.

Fundamental wave current RMS can be calculated via fundamental wave apparent power and fundamental wave voltage RMS. According to nether formula:

Fundamental wave voltage RMS: U1

Fundamental wave current RMS: I1

Fundamental wave voltage and current middle angle: Φ1

Fundamental wave active power: P1=U1*I1*cos(Φ1)

Fundamental wave reactive power: Q1=U1*I1*sin(Φ)

Fundamental wave apparent power: $S1=\sqrt{P1^2+Q1^2}=\sqrt{(U1*I1*\cos(\phi))^2+(U1*I1*\sin(\phi))^2}=U1*I1$

Fundamental wave current RMS : I1=S1/U1。

Introduction of harmonic meter:

ATT7022B selects harmonic meter mode when fundamental wave measurement enable control register EnLineFreq = 0x007812, fundamental wave measurement and harmonic measurement switch select register EnHarmonic = 0x0055AA. In the harmonic meter mode, the port CF3 output harmonic active pulse and the port CF4 output harmonic reactive pulse The corresponding parameter of fundamental wave meter is switched to parameter of harmonic meter coinstantaneous, including fundamental wave energy register is switched to harmonic energy register, fundamental wave power/voltage is switched to harmonic power/voltage.

Note: The function of fundamental wave and harmonic measurement need to be turned on via fundamental wave measurement enable control register EnLineFreq, or else ATT7022B can not measure fundamental wave and harmonic. We should close this function except when we need use it.

## §2.24 Application for 3-phase 3-wire and 3-phase 4-wire

In 3-phase 4-wire mode, ATT7022B uses 3-element measurement method. The 3-phase combined power calculated formula is:

$$P_4=\dot{U}_A\dot{I}_A+\dot{U}_B\dot{I}_B+\dot{U}_C\dot{I}_C$$

$$Q_4=\dot{U}_A\dot{I}_A\angle 90°+\dot{U}_B\dot{I}_B\angle 90°+\dot{U}_C\dot{I}_C\angle 90°$$

$$S_4=\sqrt{P_4^{\,2}+Q_4^{\,2}}$$

In 3-phase 3-wire mode, ATT7022B uses 2-element measurement method. The 3-phase combined power calculated formula is:

$$P_3=\dot{U}_{AB}\dot{I}_A+\dot{U}_{CB}\dot{I}_C$$

$$Q_3=\dot{U}_{AB}\dot{I}_A\angle 90°+\dot{U}_{CB}\dot{I}_C\angle 90°$$

$$S_3=\sqrt{P_3^{\,2}+Q_3^{\,2}}$$

In 3-phase 3-wire mode, phase B channel doesn't take part in power measurement. But ATT7022B could output phase B channel parameter solely. If we add signals to phase B voltage and current channel, we could read corresponding parameter (Pb/Qb/Sb/URmsb/IRmsb/Pfb/Pgb) in 3-phase 3-wire mode. The voltage and current signals added to phase B channel wouldn't influence normal measurement.

## §2.25 energy pulse output

ATT7022B provides 4 high-frequency pulse output: CF1/CF2/CF3/CF4.

This is energy pulse illustrated diagram:

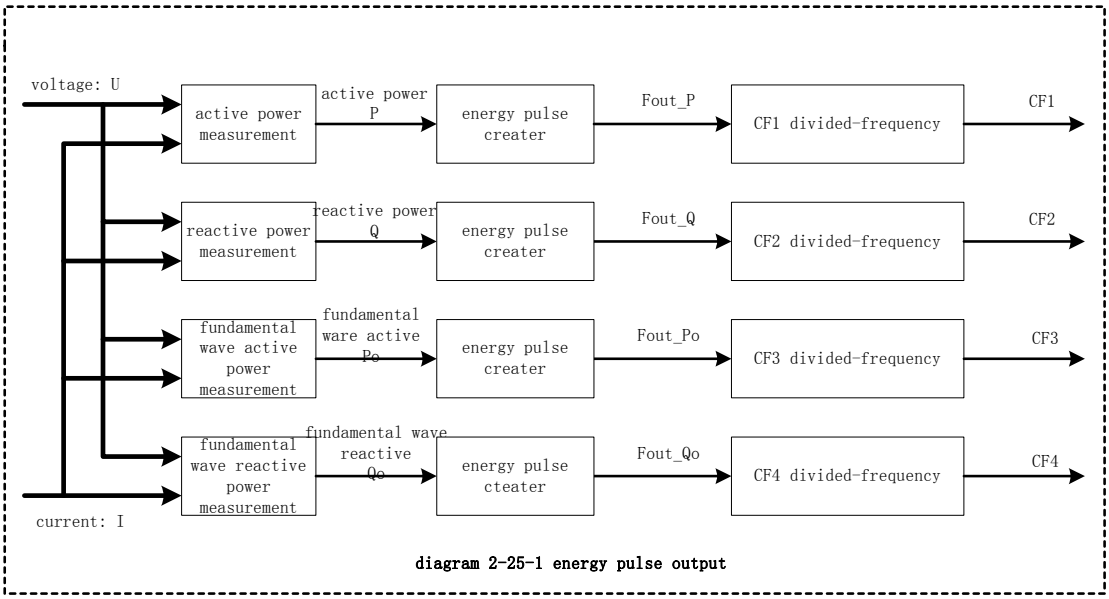



diagram 2-25-1 energy pulse output

In power measurement signal processing circuitry, the switched voltage and current signals are multiplied to get the instantaneous power, which is integrated to the time to be

turned into energy. The A/B/C phase energy is summated according to algebraic addition mode or absolute addition mode, By switching the result to frequency signal and dividing in the customized frequency division value, we get the energy pulse output signal which could be used to calibrate. The signal could be divided again to get the low-frequency pulse output which could be used to drive electromechanical step motor.

Following is the sketch map of frequency dividing while the high-frequency output constant is 64. The pulse-width of output energy pulse is 90ms. If the pulse cycle is less than 180ms, the energy pulse output duty cycle will be 1 : 1.

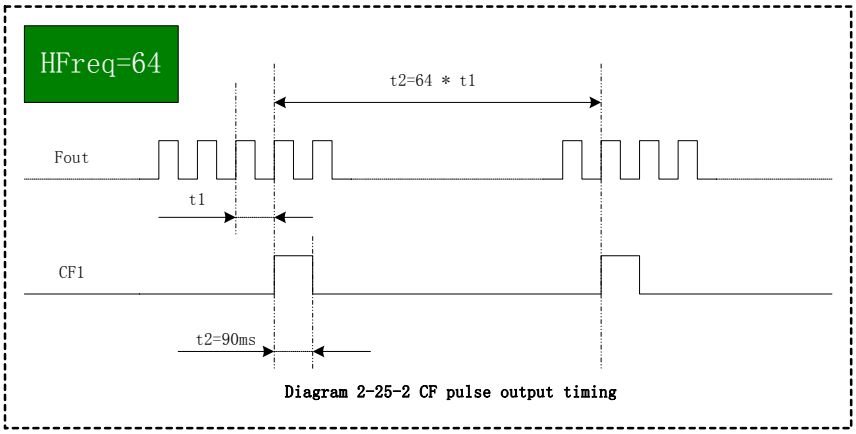



Diagram 2-25-2 CF pulse output timing

## §2.26 Parameter output registers definition

Measurement parameters output register list:

| Address | Name | Reset value | Function description |
|---|---|---|---|
| 0x00 | RESERVED | ------ | Reserved. |
| 0x01 | r_Pa | ------ | Phase A active power |
| 0x02 | r_Pb | ------ | Phase B active power |
| 0x03 | r_Pc | ------ | Phase C active power |
| 0x04 | r_Pt | ------ | 3-phase combined active power |
| 0x05 | r_Qa | ------ | Phase A reactive power |
| 0x06 | r_Qb | ------ | Phase B reactive power |
| 0x07 | r_Qc | ------ | Phase C reactive power |
| 0x08 | r_Qt | ------ | 3-phase combined reactive power |
| 0x09 | r_Sa | ------ | Phase A apparent power |
| 0x0A | r_Sb | ------ | Phase B apparent power |
| 0x0B | r_Sc | ------ | Phase C apparent power |
| 0x0C | r_St | ------ | 3-phase combined apparent power |
| 0x0D | r_URmsa | 0x000000 | Phase A voltage RMS |
| 0x0E | r_URmsb | 0x000000 | Phase B voltage RMS |
| 0x0F | r_URmsc | 0x000000 | Phase C voltage RMS |
| 0x10 | r_IRmsa | ------ | Phase A current RMS |
| 0x11 | r_IRmsb | ------ | Phase B current RMS |
| 0x12 | r_IRmsc | ------ | Phase C current RMS |

| | | | |
|---|---|---|---|
| 0x13 | r_IRmst | ------ | The RMS of phase ABC current vector sum<br>formula: $I_{rms}=\sqrt{\frac{1}{T}\int_0^T (ia+ib+ic)^2\,dt}$ |
| 0x14 | r_Pfa | ------ | Phase A power factor |
| 0x15 | r_Pfb | ------ | Phase B power factor |
| 0x16 | r_Pfc | ------ | Phase C power factor |
| 0x17 | r_Pft | ------ | 3-phase combined power factor |
| 0x18 | r_Pga | ------ | Phase A phase angle |
| 0x19 | r_Pgb | ------ | Phase B phase angle |
| 0x1A | r_Pgc | ------ | Phase C phase angle |
| 0x1B | r_Pgt | ------ | 3-phase combined phase angle |
| 0x1C | r_Freq | 0x000000 | Line frequency |
| 0x1D | RESERVED | ------ | Reserved. |
| 0x1E | r_Epa | 0x000000 | Phase A active energy |
| 0x1F | r_Epb | 0x000000 | Phase B active energy |
| 0x20 | r_Epc | 0x000000 | Phase C active energy |
| 0x21 | r_Eqt | 0x000000 | 3-phase combined active energy |
| 0x22 | r_Eqa | 0x000000 | Phase A reactive energy |
| 0x23 | r_Eqb | 0x000000 | Phase B reactive energy |
| 0x24 | r_Eqc | 0x000000 | Phase C reactive energy |
| 0x25 | r_Eqt | 0x000000 | 3-phase combined reactive energy |
| 0x26 | RESERVED | ------ | Reserved. |
| 0x27 | RESERVED | ------ | Reserved. |
| 0x28 | r_RSPIData | ------ | Last data that SPI read |
| 0x29 | r_RmsADC7 | ------ | Input signal RMS of NO. 7 ADC |
| 0x2A | r_TempD | ------ | Output of temperature sensor |
| 0x2B | r_URmst | 0x000000 | The RMS of phase ABC voltage vector sum<br>formula: $U_{rms}=\sqrt{\frac{1}{T}\int_0^T (ua+ub+uc)^2\,dt}$ |
| 0x2C | r_SFlag | | Status of phase-cut, phase sequence , and SIG |
| 0x2D | r_WSPIData1 | ------ | Last data that SPI write |
| 0x2E | r_WSPIData2 | ------ | Same to 0x2D, is last data that SPI read too |
| 0x2F | RESERVED | ------ | Reserved. |
| 0x30 | r_EFlag | 0x010000 | Status of energy register |
| 0x31 | r_Epa2 | 0x000000 | Phase A active energy, same to Epa, but would be clear to 0 after read. |
| 0x32 | r_Epb2 | 0x000000 | Phase B active energy, same to Epb, but would be clear to 0 after read. |
| 0x33 | r_Epc2 | 0x000000 | Phase C active energy, same to Epc, but would be clear to 0 after read. |

| | | | |
|---|---|---|---|
| 0x34 | r_Ept2 | 0x000000 | 3-phase combined active energy, same to Ept, but would be clear to 0 after read. |
| 0x35 | r_Eqa2 | 0x000000 | Phase A reactive energy, same to Eqa, but would be clear to 0 after read. |
| 0x36 | r_Eqb2 | 0x000000 | Phase B reactive energy, same to Eqb, but would be clear to 0 after read. |
| 0x37 | r_Eqc2 | 0x000000 | Phase C reactive energy, same to Eqc, but would be clear to 0 after read. |
| 0x38 | r_Eqt2 | 0x000000 | 3-phase combined reactive energy, same to Eqt, but would be clear to 0 after read. |
| 0x39 | RESERVED | ------ | Reserved. |
| 0x3A | RESERVED | ------ | Reserved. |
| 0x3B | RESERVED | ------ | Reserved. |
| 0x3C | r_LEFlag | 0x000000 | Status of fundamental wave energy register |
| 0x3D | r_PFlag | ------ | The direction of active and reactive power, positive is 0, negative is 1. |
| 0x3E | r_ChkSum1 | 0x043D03 | Calibration data checkout register(3-phase 4-wire mode) |
| | | 0x16BD03 | Calibration data checkout register(3-phase 3-wire mode) |
| 0x3F | r_InstADC7 | ------ | Sampling data output of No.7 ADC |
| 0x40 | r_PosEpa | 0x000000 | Positive phase A active energy register |
| 0x41 | r_PosEpb | 0x000000 | Positive phase B active energy register |
| 0x42 | r_PosEpc | 0x000000 | Positive phase C active energy register |
| 0x43 | r_PosEpt | 0x000000 | Positive 3-phase active energy register |
| 0x44 | r_NegEpa | 0x000000 | Negative phase A active energy register |
| 0x45 | r_NegEpb | 0x000000 | Negative phase B active energy register |
| 0x46 | r_NegEpc | 0x000000 | Negative phase C active energy register |
| 0x47 | r_NegEpt | 0x000000 | Negative 3-phase active energy register |
| 0x48 | r_PosEqa | 0x000000 | Positive phase A reactive energy register |
| 0x49 | r_PosEqb | 0x000000 | Positive phase B reactive energy register |
| 0x4A | r_PosEqc | 0x000000 | Positive phase C reactive energy register |
| 0x4B | r_PosEqt | 0x000000 | Positive 3-phase reactive energy register |
| 0x4C | r_NegEqa | 0x000000 | Negative phase A reactive energy register |
| 0x4D | r_NegEqb | 0x000000 | Negative phase B reactive energy register |
| 0x4E | r_NegEqc | 0x000000 | Negative phase C reactive energy register |
| 0x4F | r_NegEqt | 0x000000 | Negative 3-phase reactive energy register |
| 0x50 | r_LineEpa | 0x000000 | Phase A fundamental wave active energy |
| 0x51 | r_LineEpb | 0x000000 | Phase B fundamental wave active energy |
| 0x52 | r_LineEpc | 0x000000 | Phase C fundamental wave active energy |
| 0x53 | r_LineEpt | 0x000000 | 3-phase fundamental wave active energy |
| 0x54 | r_LineEqa | 0x000000 | Phase A fundamental wave reactive energy |
| 0x55 | r_LineEqb | 0x000000 | Phase B fundamental wave reactive energy |

| | | | |
|---|---|---|---|
| 0x56 | r_LineEqc | 0x000000 | Phase C fundamental wave reactive energy |
| 0x57 | r_LineEqt | 0x000000 | 3-phase fundamental wave reactive energy |
| 0x58 | RESERVED | ------ | Reserved. |
| 0x59 | RESERVED | ------ | Reserved. |
| 0x5A | RESERVED | ------ | Reserved. |
| 0x5B | RESERVED | ------ | Reserved. |
| 0x5C | r_YUaUb | 0x000000 | Voltage middle angle in Ua and Ub |
| 0x5D | r_YUaUc | 0x000000 | Voltage middle angle in Ua and Uc |
| 0x5E | r_YUbUc | 0x000000 | Voltage middle angle in Ub and Uc |
| 0x5F | r_ChkSum2 | 0x043D03 | Same to 0x3E. Calibration data checkout register(3-phase 4-wire mode) |
| | | 0x16BD03 | Same to 0x3E. Calibration data checkout register(3-phase 3-wire mode) |
| 0x60 | r_PosEpa2 | 0x000000 | Positive phase A active energy register, same to PosEpa, but would be clear to 0 after read. |
| 0x61 | r_PosEpb2 | 0x000000 | Positive phase B active energy register, same to PosEpb, but would be clear to 0 after read. |
| 0x62 | r_PosEpc2 | 0x000000 | Positive phase C active energy register, same to PosEpc, but would be clear to 0 after read. |
| 0x63 | r_PosEpt2 | 0x000000 | Positive 3-phase combined active energy register, same to PosEpt, but would be clear to 0 after read. |
| 0x64 | r_NegEpa2 | 0x000000 | Negative phase A active energy register, same to NegEpa, but would be clear to 0 after read. |
| 0x65 | r_NegEpb2 | 0x000000 | Negative phase B active energy register, same to NegEpb, but would be clear to 0 after read. |
| 0x66 | r_NegEpc2 | 0x000000 | Negative phase C active energy register, same to NegEpc, but would be clear to 0 after read. |
| 0x67 | r_NegEpt2 | 0x000000 | Negative 3-phase combined active energy register, same to NegEpt, but would be clear to 0 after read. |
| 0x68 | r_PosEqa2 | 0x000000 | Positive phase A reactive energy register, same to PosEqa, but would be clear to 0 after read. |
| 0x69 | r_PosEqb2 | 0x000000 | Positive phase B reactive energy register, same to PosEqb, but would be clear to 0 after read. |
| 0x6A | r_PosEqc2 | 0x000000 | Positive phase C reactive energy register, same to PosEqc, but would be clear to 0 after read. |
| 0x6B | r_PosEqt2 | 0x000000 | Positive 3-phase combined reactive energy register, same to PosEqt, but would be clear to 0 after read. |
| 0x6C | r_NegEqa2 | 0x000000 | Negative phase A reactive energy register, same to NegEqa, but would be clear to 0 after read. |

| | | | |
|---|---|---|---|
| 0x6D | r_NegEqb2 | 0x000000 | Negative phase B reactive energy register, same to NegEqb, but would be clear to 0 after read. |
| 0x6E | r_NegEqc2 | 0x000000 | Negative phase C reactive energy register, same to NegEqc, but would be clear to 0 after read. |
| 0x6F | r_NegEqt2 | 0x000000 | Negative 3-phase combined reactive energy register, same to NegEqt, but would be clear to 0 after read. |
| 0x70 | r_LineEpa2 | 0x000000 | Phase A fundamental wave active energy, same to LineEpa, but would be clear to 0 after read. |
| 0x71 | r_LineEpb2 | 0x000000 | Phase B fundamental wave active energy, same to LineEpb, but would be clear to 0 after read. |
| 0x72 | r_LineEpc2 | 0x000000 | Phase C fundamental wave active energy, same to LineEpc, but would be clear to 0 after read. |
| 0x73 | r_LineEpt2 | 0x000000 | 3-phase combined fundamental wave active energy, same to LineEpt, but would be clear to 0 after read. |
| 0x74 | r_LineEqa2 | 0x000000 | Phase A fundamental wave reactive energy, same to LineEqa, but would be clear to 0 after read. |
| 0x75 | r_LineEqb2 | 0x000000 | Phase B fundamental wave reactive energy, same to LineEqb, but would be clear to 0 after read. |
| 0x76 | r_LineEqc2 | 0x000000 | Phase C fundamental wave reactive energy, same to LineEqc, but would be clear to 0 after read. |
| 0x77 | r_LineEqt2 | 0x000000 | 3-phase combined fundamental wave reactive energy, same to LineEqt, but would be clear to 0 after read. |
| 0x78 | RESERVED | ------ | Reserved. |
| 0x79 | RESERVED | ------ | Reserved. |
| 0x7A | RESERVED | ------ | Reserved. |
| 0x7B | RESERVED | ------ | Reserved. |
| 0x7C | RESERVED | ------ | Reserved. |
| 0x7D | RESERVED | ------ | Reserved. |
| 0x7E | RESERVED | ------ | Reserved. |
| 0x7F | RESERVED | ------ | Reserved. |

## §2.27 Parameter output registers specification

### 2.27.1 power register (Address: 0x01～0x0C)

Register list: (refresh time is about 1/3 second. For the first time, the correct value would be available after 650ms.)

| Addr | 0x01 | 0x02 | 0x03 | 0x04 | 0x05 | 0x06 | 0x07 | 0x08 | 0x09 | 0x0A | 0x0B | 0x0C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Reg** | Pa | Pb | Pc | Pt | Qa | Qb | Qc | Qt | Sa | Sb | Sc | St |

ATT7022B power register uses supplementary code, the MSB is symbol bit. We can judge current quadrant according to the direction of active and reactive power in ATT7022B power register. Because of apparent power always $\geqslant 0$, so the symbol bit of apparent power is 0 at all time.

The formats of power register:

For each single phase of A/B/C: the power parameter is X

X: 24bits, supplementary code

If it is greater than 2^23, then XX = X-2^24

Else XX=X

The real power is: XXX=XX*2^15/2^23

For 3-phase combined data: the power parameter is T

T: 24bits, supplementary code

If it is greater than 2^23, then TT = T-2^24

Else TT=T

The real power is: TTT=TT*2^17/2^23

The unit of power is Watt (w), which is relevant to pulse constant. Above mentioned real power is based on 3200 imp/kwh; if the pulse constant is set as EC, then the real power should be the product of TTT and 3200/EC.

### 2.27.2 RMS register (Address: 0x0D～0x13、0x29、0x2B)

Register list: (refresh time is about 1/3 second. For the first time, the correct value would be available after 650ms.)

| Addr | 0x0D | 0x0E | 0x0F | 0x10 | 0x11 | 0x12 |
|---|---|---|---|---|---|---|
| **Reg** | URmsa | URmsb | URmsc | IRmsa | IRmsb | IRmsc |
| Addr | 0x13 | 0x29 | 0x2B | | | |
| **Reg** | IRmst | RmsADC7 | URmst | | | |

ATT7022B RMS register uses supplementary code and the MSB is symbol bit. Since RMS is always $\geqslant 0$, the symbol bit of RMS is 0 at all time.

Vrms: 24bits, supplementary code

The real voltage RMS is: Urms=Vrms*2^10/2^23

Unit is Volt (V) or Ampere (A).

### 2.27.3 power factor register (Address:0x14～0x17)

c

| Addr | 0x14 | 0x15 | 0x16 | 0x17 |
|---|---|---|---|---|
| **Reg** | Pfa | Pfb | Pfc | Pft |

ATT7022B power factor register uses supplementary code, the MSB is symbol bit. The symbol bit of power factor is decided by symbol bit of reactive power, please refer to power factor measurement section: 2.13.

PF: 24bits, supplementary code

If PF > 2^23, then PFF=PF-2^24

Else PFF=PF

The real power factor is: pf = PFF/2^23

### 2.27.4 phase angle register (Address: 0x18～0x1B)

Register list: (refresh time is about 1/3 second. For the first time, correct value would be available after 650ms.)

| Addr | 0x18 | 0x19 | 0x1A | 0x1B |
|---|---|---|---|---|
| **Reg** | Pga | Pgb | Pgc | Pgt |

ATT7022B phase angle register uses supplementary code, the MSB is symbol bit, denotes the middle angle in -90º～+90º.

Θ: 24bits, supplementary code

If θ > 2^23, then α=θ-2^24

Else α=θ

The real phase angle is:

Pg = (α/2^23)*2*180/pi (angle)

Or Pg = (α/2^23)*2 (radian)

### 2.27.5 line frequency register (Address: 0x1C)

ATT7022B line frequency register uses supplementary code format, the MSB is symbol bit, the symbol bit is 0 at all time.

Freq: 24bits, supplementary code

The real frequency is: f = Freq*2^10/2^23

Unit: Hz

### 2.27.6 energy register (Adress: 0x1E～0x25、0x31～0x38、0x40～0x4F、0x60～0x6F)

Register list:

| Addr | 0x1E | 0x1F | 0x20 | 0x21 | 0x22 | 0x23 | 0x24 | 0x25 |
|---|---|---|---|---|---|---|---|---|
| **Reg** | Epa | Epb | Epc | Ept | Eqa | Eqb | Eqc | Eqt |
| Addr | 0x31 | 0x32 | 0x33 | 0x34 | 0x35 | 0x36 | 0x37 | 0x38 |

| **Reg** | Epa2 | Epb2 | Epc2 | Ept2 | Eqa2 | Eqb2 | Eqc2 | Eqt2 |
|---|---|---|---|---|---|---|---|---|
| Addr | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 | 0x45 | 0x46 | 0x47 |
| **Reg** | PosEpa | PosEpb | PosEpc | PosEpt | NegEpa | NegEpb | NegEpc | NegEpt |
| Addr | 0x48 | 0x49 | 0x4A | 0x4B | 0x4C | 0x4D | 0x4E | 0x4F |
| **Reg** | PosEqa | PosEqb | PosEqc | PosEqt | NegEqa | NegEqb | NegEqc | NegEqt |
| Addr | 0x60 | 0x61 | 0x62 | 0x63 | 0x64 | 0x65 | 0x66 | 0x67 |
| **Reg** | PosEpa2 | PosEpb2 | PosEpc2 | PosEpt2 | NegEpa2 | NegEpb2 | NegEpc2 | NegEpt2 |
| Addr | 0x68 | 0x69 | 0x6A | 0x6B | 0x6C | 0x6D | 0x6E | 0x6F |
| **Reg** | PosEqa2 | PosEqb2 | PosEqc2 | PosEqt2 | NegEqa2 | NegEqb2 | NegEqc2 | NegEqt2 |

ATT7022B provides two kinds of energy registers, one is accumulated type, and the other is clear after reading type. The clear after reading energy register has an append ‘2’ as identifier. There is no influence to clear after reading type energy register if we read accumulated type energy register. But if we read clear after reading type energy register, the accumulated type energy register would be cleared to 0 too at next energy refresh. The range of increased energy register is 0x000000 ~ 0xFFFFFF. If energy overflows from 0xFFFFFF to 0x000000, the overflow flag would be brought. Please refer to specification about status of energy register: 2.27.9.

Energy register: 24bits, unsigned data.

The data is based on the pulse constant. For example, if the pulse constant is set to 3200 imp/kwh, then the unit of data for these energy registers is 1/3200kwh.

### 2.27.7 temperature sensor data register (Address: 0x2A)

temperature sensor data output register:

| | Bit23..Bit8 | TM7 | TM6 | TM5 | TM4 | TM3 | TM2 | TM1 | TM0 |
|---|---|---|---|---|---|---|---|---|---|
| Data | Xxx | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TM:24bits, the low 8 bits is active.

If TM > 128, then TMM=TM-256

Else TMM=TM

After external MCU read this register and switch according to above mentioned, the real temperature could be achieved via formula: TC-TMM, TC is temperature calibration value.

### 2.27.8 status flag register (Address: 0x2C)

SFlag bit definition:

| | Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
|---|---|---|---|---|---|---|---|---|
| **Def** | --- | --- | --- | --- | --- | --- | --- | --- |
| | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| **Def** | --- | --- | --- | --- | Cstart | Bstart | Astart | --- |
| | Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| **Def** | SIG | --- | --- | Iorder | Uorder | PC | PB | PA |

Bit00: =1 denotes phase A power failure

Bit01: =1 denotes phase B power failure

Bit02: =1 denotes phase C power failure

Bit03: =1 denotes voltage phase sequence is error

Bit04: =1 denotes current phase sequence is error

Bit07: SIG would go low when ATT7022B power on reset or unconventional reset, at the same time this bit (SFlag.7) is set to 1; After the host MCU sends calibration data via SPI, SIG would goes high immediately, and SFlag.7 would be cleared to 0 simultaneous. So the Bit07 in SFlag register is synchronous with SIG signal.

Bit09: =1 denotes phase A is in creep protection state.

Bit10: =1 denotes phase B is in creep protection state.

Bit11: =1 denotes phase C is in creep protection state.

### 2.27.9 status of energy register (Address: 0x30)

This register would be cleared to 0 automatically after read.

| | |
|---|---|
| Bit0~2: | Phase A, B, C positive active energy register overflow. |
| Bit3: | 3-phase positive active energy register overflow. |
| Bit4~6: | Phase A, B, C positive reactive energy register overflow. |
| Bit7: | 3-phase positive reactive energy register overflow. |
| Bit8~10: | Phase A, B, C negative active energy register overflow. |
| Bit11: | 3-phase negative active energy register overflow. |
| Bit12~14: | Phase A, B, C negative reactive energy register overflow. |
| Bit15: | 3-phase negative reactive energy register overflow. |
| Bit16: | Calibration request after system reset. This bit will be set after each system reset. |

### 2.27.10 active and reactive power direction register (Address: 0x3D)

Power direction indication register (PFlag): used to indicate the direction of phase A, B, C, and 3-phase combined active and reactive power.

Bit0-3: denotes the direction of phase A, B, C, and 3-phase combined active power, 0 is positive and 1 is negative.

Bit4-7: denotes the direction of phase A, B, C, and 3-phase combined reactive power, 0 is positive and 1 is negative.

### 2.27.11 Calibration data checksum register (Address: 0x3E、0x5F)

ATT7022B provides two special registers: ChkSum1 and ChkSum2, which are used to conserve the checksum value of all calibration data. External MCU can use them to examine calibration data's error. The checksum value is summation of all calibration data from 0x01 to 0x3F.

After external MCU has written the calibration data, ATT7022B calculate and update

the checksum in 1/3 second.

Note: ChkSum1 and ChkSum2 are irrelative, but the definition is identical.

### 2.27.12 No.7 ADC sampling output register (Address: 0x3F)

This is sampling data output of No.7 ADC, low 16 bits active. This register uses 16-bits supplementary code format, the MSB is symbol bit. The sampling speed is 3.2 KHz.

### 2.27.13 Voltage middle angle register (Address: 0x5C～0x5E)

The voltage phase angle measurement accuracy is about 5º.

There are 3 registers: YUaUb/YUaUc/YUbUc, which denote phase AB/AC/BC voltage middle angle respectively.

Middle angle formula: YUaUb*2^10/2^23=YUaUb/2^13。

### 2.27.14 fundamental wave energy register (Address: 0x50～0x57、0x70～0x77)

Register list:

| Address | Name | Reset value | Function description |
|---|---|---|---|
| 0x50 | R_LineEpa | 0x000000 | Phase A fundamental wave active energy |
| 0x51 | R_LineEpb | 0x000000 | Phase B fundamental wave active energy |
| 0x52 | R_LineEpc | 0x000000 | Phase C fundamental wave active energy |
| 0x53 | R_LineEpt | 0x000000 | 3-phase fundamental wave active energy |
| 0x54 | R_LineEqa | 0x000000 | Phase A fundamental wave reactive energy |
| 0x55 | R_LineEqb | 0x000000 | Phase B fundamental wave reactive energy |
| 0x56 | r_LineEqc | 0x000000 | Phase C fundamental wave reactive energy |
| 0x57 | r_LineEqt | 0x000000 | 3-phase fundamental wave reactive energy |
| 0x70 | r_LineEpa2 | 0x000000 | Phase A fundamental wave active energy, same to LineEpa, but would be clear to 0 after read. |
| 0x71 | r_LineEpb2 | 0x000000 | Phase B fundamental wave active energy, same to LineEpb, but would be clear to 0 after read. |
| 0x72 | r_LineEpc2 | 0x000000 | Phase C fundamental wave active energy, same to LineEpc, but would be clear to 0 after read. |
| 0x73 | r_LineEpt2 | 0x000000 | 3-phase combined fundamental wave active energy, same to LineEpt, but would be clear to 0 after read. |
| 0x74 | r_LineEqa2 | 0x000000 | Phase A fundamental wave reactive energy, same to LineEqa, but would be clear to 0 after read. |
| 0x75 | r_LineEqb2 | 0x000000 | Phase B fundamental wave reactive energy, same to LineEqb, but would be clear to 0 after read. |

| | | | |
|---|---|---|---|
| 0x76 | r_LineEqc2 | 0x000000 | Phase C fundamental wave reactive energy, same to LineEqc, but would be clear to 0 after read. |
| 0x77 | r_LineEqt2 | 0x000000 | 3-phase combined fundamental wave reactive energy, same to LineEqt, but would be clear to 0 after read. |

In fundamental wave meter mode, these registers conserve fundamental wave active and reactive energy, please refer to section 2.27.6.

### 2.27.15 RMS apparent energy register (Address: 0x50～0x57、0x70～0x77)

Register list:

| Address | Name | Reset value | Function description |
|---|---|---|---|
| 0x50 | r_LineEpa | 0x000000 | Phase A RMS apparent energy |
| 0x51 | r_LineEpb | 0x000000 | Phase B RMS apparent energy |
| 0x52 | r_LineEpc | 0x000000 | Phase C RMS apparent energy |
| 0x53 | r_LineEpt | 0x000000 | 3-phase RMS apparent energy |
| 0x54 | r_LineEqa | 0x000000 | ------ |
| 0x55 | r_LineEqb | 0x000000 | ------ |
| 0x56 | r_LineEqc | 0x000000 | ------ |
| 0x57 | r_LineEqt | 0x000000 | ------ |
| 0x70 | r_LineEpa2 | 0x000000 | Phase A RMS apparent energy, same to LineEpa, but would be clear to 0 after read. |
| 0x71 | r_LineEpb2 | 0x000000 | Phase B RMS apparent energy, same to LineEpb, but would be clear to 0 after read. |
| 0x72 | r_LineEpc2 | 0x000000 | Phase C RMS apparent energy, same to LineEpc, but would be clear to 0 after read. |
| 0x73 | r_LineEpt2 | 0x000000 | 3-phase combined RMS apparent energy, same to LineEpt, but would be clear to 0 after read. |
| 0x74 | r_LineEqa2 | 0x000000 | ------ |
| 0x75 | r_LineEqb2 | 0x000000 | ------ |
| 0x76 | r_LineEqc2 | 0x000000 | ------ |
| 0x77 | r_LineEqt2 | 0x000000 | ------ |

In RMS apparent energy measurement mode, these registers conserve RMS apparent energy, please refer to section 2.27.6.

### 2.27.16 PQS apparent energy register (Address: 0x50～0x57、0x70～0x77)

Register list:

| Address | Name | Reset value | Function description |
|---|---|---|---|
| 0x50 | r_LineEpa | 0x000000 | Phase A PQS apparent energy |
| 0x51 | r_LineEpb | 0x000000 | Phase B PQS apparent energy |
| 0x52 | r_LineEpc | 0x000000 | Phase C PQS apparent energy |
| 0x53 | r_LineEpt | 0x000000 | ------ |

| | | | |
|---|---|---|---|
| 0x54 | r_LineEqa | 0x000000 | ------ |
| 0x55 | r_LineEqb | 0x000000 | ------ |
| 0x56 | r_LineEqc | 0x000000 | ------ |
| 0x57 | r_LineEqt | 0x000000 | 3-phase PQS apparent energy |
| 0x70 | r_LineEpa2 | 0x000000 | Phase A PQS apparent energy, same to LineEpa, but would be clear to 0 after read. |
| 0x71 | r_LineEpb2 | 0x000000 | Phase B PQS apparent energy, same to LineEpb, but would be clear to 0 after read. |
| 0x72 | r_LineEpc2 | 0x000000 | Phase C PQS apparent energy, same to LineEpc, but would be clear to 0 after read. |
| 0x73 | r_LineEpt2 | 0x000000 | ------ |
| 0x74 | r_LineEqa2 | 0x000000 | ------ |
| 0x75 | r_LineEqb2 | 0x000000 | ------ |
| 0x76 | r_LineEqc2 | 0x000000 | ------ |
| 0x77 | r_LineEqt2 | 0x000000 | 3-phase combined PQS apparent energy, same to LineEpt, but would be clear to 0 after read. |

In PQS apparent energy measurement mode, these registers conserve PQS apparent energy, please refer to section 2.27.6.

### 2.27.17 Status of fundamental wave energy register (Address: 0x3C)

Bit0: =1 denotes LineEpa(0x50) register overflow.
Bit1: =1 denotes LineEpb(0x51) register overflow.
Bit2: =1 denotes LineEpc(0x52) register overflow.
Bit3: =1 denotes LineEpt(0x53) register overflow.
Bit4: =1 denotes LineEqa(0x54) register overflow.
Bit5: =1 denotes LineEqb(0x55) register overflow.
Bit6: =1 denotes LineEqc(0x56) register overflow.
Bit7: =1 denotes LineEqt(0x57) register overflow.
This register would be cleared to 0 automatically after read.

### 2.27.18 SPI read checkout register (Address: 0x28)

This register conserves the last read data by SPI. This register could be used to checkout when SPI read data.

### 2.27.19 SPI write checkout register (Address: 0x2D、0x2E)

These registers conserve the last written data by SPI. These registers could be used to checkout when SPI write data.

Noticed: WSPIData1 and WSPIData2 are irrelative, but the definition is identical.

# Chapter 3 Calibration

## §3.1 Software calibration

ATT7022B supplies software calibration. After calibrated, the active accuracy can achieve 0.5s and reactive accuracy can achieve 2s.

Power calibration is completed by the active power gain calibration and the phase compensation.

The active power is calibrated for one phase at a time. ATT7022B provides Iregchg register, which could set compensation subsection region, as illustrated in the nether figure.

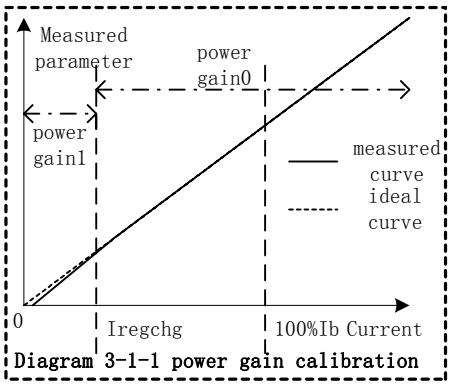



Diagram 3-1-1 power gain calibration

We should set Iregchg according to actual application. After Iregchg is set, we need calibrate active power gain respectively to the two current ranges. If the register Iregchg is set to zero, only one current range is used for the active power gain calibration.

The phase difference between voltage and current channel is compensated with these phase calibration registers. The ATT7022B is calibrated for phase compensation at five current point to cover the complete current range, which is very effective and user friendly, as illustrated in the nether figure.

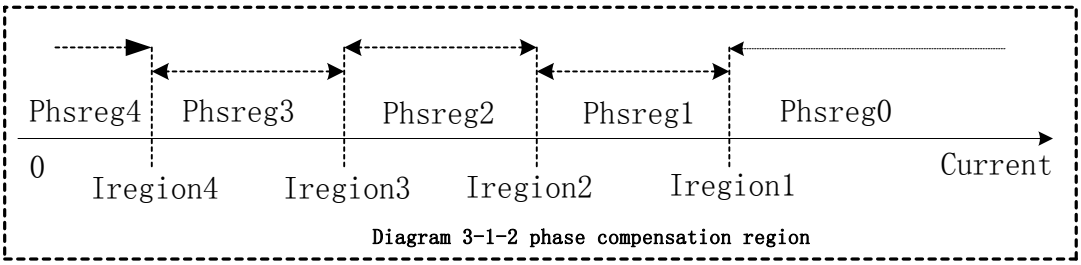



Diagram 3-1-2 phase compensation region

In fact, only two current points are required for the accuracy class 1 and 0.5 when the low phase shifts CT's. More current points are required for the accuracy class 0.2 or higher.

It is recommended that the phase compensation is performed in 0.5L after the active power gain calibration has been performed in power factor 1.0.

Voltage and current RMS are calibrated by the register in the ATT7022B. Correlative calculated formula please refers to the latter detailed specification.

ATT7022B high-frequency pulse output (calibration pulse rate) can be set by the register HFConst. Starting current can be set by the register Istartup.

## §3.2 Calibration register definition

| Address | Name | Reset value | Function description |
|---|---|---|---|
| 0x00 | RESERVED | ------ | Reserved. |
| 0x01 | RESERVED | 0x000000 | Reserved. |
| 0x02 | w_Iregion1 | 0x000000 | Phase calibration region 1 setup |
| 0x03 | w_Iregion2 | 0x000000 | Phase calibration region 2 setup |
| 0x04 | w_Iregion3 | 0x000000 | Phase calibration region 3 setup |
| 0x05 | w_Iregion4 | 0x000000 | Phase calibration region 4 setup |
| 0x06 | w_PgainA0 | 0x000000 | Phase A active power gain 0 |
| 0x07 | w_PgainB0 | 0x000000 | Phase B active power gain 0 |
| 0x08 | w_PgainC0 | 0x000000 | Phase C active power gain 0 |
| 0x09 | w_PgainA1 | 0x000000 | Phase A active power gain 1 |

| | | | |
|---|---|---|---|
| 0x26 | w_IgainA | 0x000000 | Phase A current gain |
| 0x27 | w_IgainB | 0x000000 | Phase B current gain |
| 0x28 | w_IgainC | 0x000000 | Phase C current gain |
| 0x29 | w_FailVoltage | 0x068000 | Threshold value of power failure (3-phase 4-wire mode) |
| | | 0x190000 | Threshold value of power failure (3-phase 3-wire mode) |
| 0x2A | w_EAddMode | 0x000000 | Calculating mode of 3 phase energy (sum in algebra/ absolute) |
| 0x2B | w_GainAdc7 | 0x000000 | RMS calibration to No.7 ADC |
| 0x2C | w_GCtrlT7Adc | 0x000003 | Temperature/No.7 ADC select control |
| 0x2D | w_EnLineFreq | 0x000000 | Fundamental wave measurement enable control |
| 0x2E | w_EnUAngle | 0x000000 | Voltage middle angle measurement enable control |
| 0x2F | w_SelectPQSU | 0x000000 | Fundamental wave voltage power output select |
| 0x30 | w_EnDtIorder | 0x000000 | Current phase sequence detecting enable control |
| 0x31 | w_LineFreqPg | 0x0020C4 | Fundamental wave power calibration |
| 0x32 | RESERVED | 0x040000 | Reserved. |
| 0x33 | RESERVED | 0x000000 | Reserved. |
| 0x34 | RESERVED | 0x000000 | Reserved. |
| 0x35 | RESERVED | 0x000000 | Reserved. |
| 0x36 | RESERVED | 0x000000 | Reserved. |
| 0x37 | RESERVED | 0x000000 | Reserved. |
| 0x38 | RESERVED | 0x000000 | Reserved. |
| 0x39 | RESERVED | 0x000000 | Reserved. |
| 0x3A | RESERVED | 0x000000 | Reserved. |
| 0x3B | RESERVED | 0xF99999 | Reserved. |
| 0x3C | w_EnHarmonic | 0x000000 | Fundamental wave measurement and harmonic measurement switched select |
| 0x3D | RESERVED | 0x000000 | Reserved. |
| 0x3E | w_HFDouble | 0x000000 | Pulse constant reduplication select |
| 0x3F | w_UADCPga | 0x000000 | Voltage channel ADC gain select |

## §3.3 Calibration register specification

### 3.3.1 Calibration pulse rate: HFConst (Address: 0x20)

The frequency for the meter calibration can be selected by the register HFConst. The data written to HFConst can not be greater than 0x000D00.

Enactment:

High-frequency pulse constant: EC
Rated input voltage: Un
Rated input current: Ib
Voltage input channel signal: Vu
Current input channel signal: Vi
ATT7022B gain: G

HFConst calculated formula:

$$\text{HFConst}= INT\left[5760000000\times\frac{G\times G\times V_u\times V_i}{U_n\times I_b\times EC}\right]$$

Note: INT[] is the round function. For example: INT[2.28]=2.

### 3.3.2 Active power calibration region setup register: Iregchg (Address: 0x1E)

Normally we don't need to separate region for active power calibration for accuracy 0.5S and 1S.

When setting active power calibration region, the corresponding input signal voltage value of region point current must be less than 35mv, or else the overflow error would be brought.

As known:

Active power calibration region: Ig (Ig<0.035)
Gain: G

Formula:

Iregchg = INT[G*Ig*$2^{23}$]

### 3.3.3 power gain calibration register: Pgain (Address: 0x06～0x0B)

Power gain is calibrated in power factor cos(Φ)=1.

If the active power calibration region setup register (Iregchg) is not zero, active power gain calibration must be performed at two current ranges (I>Iregchg and I<Iregchg) to compute the power gain. Pgain0 is the active power to Imax (I>Iregchg), and Pgain1 is the range I<Iregchg.

If the register Iregchg is set to zero, we only need calibrate active power gain in 100%Ib, then write the calibration data to Pgain0 and Pgain1 simultaneous.

As known:

The error from standard meter: err

Formula:

$$\text{Pgain}=\frac{-err}{1+err}$$

If Pgain >= 0，then Pgain = INT[Pgain*$2^{23}$]

Else if Pgain < 0，then Pgain = INT[$2^{24}$+Pgain*$2^{23}$]

Note: err could be read from standard meter, or be achieved via calculating according to nether formula:

$$err=\frac{ATT7022B\ \text{measured energy}-\text{true energy}}{\text{true energy}}\times 100\%$$

### 3.3.4 Phase calibration region setup register: Iregion (Address: 0x02～0x05)

The ATT7022B could be calibrated for phase compensation at maximum five current points to cover the complete current range.

As known:

Current region: Is

Gain: G

Formula:

Iregion = INT[G*Is*$2^{23}$]

Only two phase compensation region are required for the accuracy class 1 and class 0.5, thus only the register Iregion4 should be used, and the Iregion1/2/3 should be set to zero.

If set 2 phase compensation region, we must implement phase compensation in I>=Iregion4 and I<Iregion4 respectively. The phase compensation coefficient for the high current range (I>=Iregion4) should be set to the registers Phsreg0/1/2/3, and the phase compensation coefficient for the low current range (I<Iregion4) should be set to the register Phsreg4.

### 3.3.5 phase calibration register: Phsreg (Address: 0x0C～0x1A)

PhsregA0、PhsregA1、PhsregA2、PhsregA3、PhsregA4

PhsregB0、PhsregB1、PhsregB2、PhsregB3、PhsregB4

PhsregC0、PhsregC1、PhsregC2、PhsregC3、PhsregC4

These registers stand for region Reg0、Reg1、Reg2、Reg3、Reg4 respectively.

After active power calibration have been completed for the phase in power factor cos(Φ)=1., phase calibration can be proecessed and it should be processed in 0.5 lagging (cos(Φ)=0.5).

As known:

The error from standard meter in 0.5L: err

Phase calibration formula:

Θ = acos((1+err)*0.5)-π/3

If θ >= 0，Phsreg = INT[θ*$2^{23}$]

Else if θ < 0， Phsreg = INT[$2^{24}$+θ*$2^{23}$]

### 3.3.6 voltage RMS calibration register: Ugain(Address: 0x1B～0x1D)

When Ugain=0, the real input voltage RMS Ur can be read from the standard meter and DataU is the value of measured voltage channel RMS register which is read from SPI port.

As known:

The real input voltage RMS: Ur

The measured voltage RMS: Urms = DataU*$2^{10}$/$2^{23}$

Formula:

Ugain = Ur/Urms-1

If Ugain >= 0, then Ugain = INT[Ugain*$2^{23}$]

Else if Ugain < 0, then Ugain = INT[$2^{24}$+Ugain*$2^{23}$]

### 3.3.7 current RMS calibration register: Igain (Addrress: 0x26～0x28)

When Igain=0, the real input current RMS Ir can be read from the standard meter, and DataI is the value of measured current channel RMS register which is read from SPI port.

As known:

The real input current RMS: Ir

The measured current RMS: Irms = DataI*$2^{10}$/$2^{23}$

Formula:

Igain = Ir/Irms-1

If Igain >= 0, then Igain = INT[Igain*$2^{23}$]

Else if Igain < 0, then Igain = INT[$2^{24}$+Igain*$2^{23}$]

Note:

ATT7022B can provide RMS parameter for A/B/C 3 phase current vector summation: IRmst. For the accuracy of IRmst, the nether current RMS calibration method is recommended.

When input rated current Ib, the sampling voltage in current channel is about 100mv, the read parameter from current RMS register is about 60A in Igain=0, at this time the current RMS should be calibrate to N*Ib, the real RMS could be get via (MCU read ATT7022 current RMS) / (N). N*Ib should near 60A to the best of its abilities.

For example, if rated current Ib = 1.5A, then N = 40. If rated current Ib = 5A, then N = 12.

### 3.3.8 starting current setup register: Istartup (Address: 0x1F)

As known:

Starting current select Io

Gain: G

Formula:

Istartup=INT[G*Io*$2^{23}$]

### 3.3.9 Threshold value of power failure setting register: FailVoltage (Address: 0x29)

Threshold value of power failure is setup according to calibrated voltage.

Formula: FailVoltage = Un*$2^{13}$*D

Un: denotes calibrated rated voltage

D: denotes power failure voltage value, is a percent

For example, ① In 3-phase 4-wire, calibrated rated voltage Un is 220v, power failure voltage value is 10%, then FailVoltage = 220*$2^{13}$*10% = 0x02C000. Scilicet when 0x02C000 was written to threshold value of power failure setting register, if input voltage is less than Un*10% (22v), power failure indication would be brought. ② In 3-phase 3-wire, calibrated rated voltage Un is 100v, power failure voltage value is 60%, then FailVoltage = 100*$2^{13}$*60% = 0x078000. Scilicet when 0x078000 was written to threshold value of power failure setting register, if input voltage is less than Un*60% (60v), power failure indication would be brought.

### 3.3.10 3 phase energy addition mode select register: EAddMode (Address: 0x2A)

As default, EAddMode[Bit0] = 0, in 3-phase 4-wire, denotes absolute addition mode; in 3-phase 3-wire, denotes algebraic addition mode.

When EAddMode[Bit0] = 1, in 3-phase 4-wire, denotes algebraic addition mode; in 3-phase 3-wire, denotes absolute addition mode.

### 3.3.11 Temperature/No.7 ADC select control register: GCtrlT7Adc (Address: 0x2C)

ATT7022B has a built-in temperature sensor, and extends a separate ADC which could be used to detect neutral-line current. These could be enabled via register GCtrlT7Adc.

GCtrlT7Adc[bit0] is used to enable No.7 ADC, Bit0=1 denotes opening No.7 ADC, Bit0=0 denotes closing No.7 ADC.

GCtrlT7Adc[bit2/bit1] is used tp enable temperature sensor, only Bit2/1=10 denotes opening temperature sensor, Bit2/1=00/01/11 denotes closing temperature sensor.

| GCtrlT7Adc | | | | Temperature sensor | No.7 ADC |
|---|---|---|---|---|---|
| Bit23..3 | Bit2 | Bit1 | Bit0 | | |
| ------ | 0 | 0 | 0 | OFF | OFF |
| ------ | 0 | 0 | 1 | OFF | ON |
| ------ | 0 | 1 | 0 | OFF | OFF |
| ------ | 0 | 1 | 1 | OFF | ON |

| | | | | | |
|---|---|---|---|---|---|
| ------ | 1 | 0 | 0 | ON | OFF |
| ------ | 1 | 0 | 1 | ON | ON |
| ------ | 1 | 1 | 0 | OFF | OFF |
| ------ | 1 | 1 | 1 | OFF | ON |

### 3.3.12 No.7 ADC RMS calibration register: GainAdc7 (Address: 0x2B)

No.7 ADC usually is used to detect neutral-line current. ATT7022B can also calibrate neutral-line current.

When GainAdc7=0, the real input current RMS I7r can be read from the more precise current RMS meter, DataI7 is the measured current RMS register which is read from the SPI port.

As known:

the real input current RMS: I7r

the measured current RMS: I7rms = DataI7*$2^{10}/2^{23}$

Fromula:

GainAdc7 = I7r/I7rms-1

If GainAdc7 >= 0, then GainAdc7 = INT[GainAdc7*$2^{23}$]

Else if GainAdc7 < 0, then GainAdc7 = INT[$2^{24}$+ GainAdc7*$2^{23}$]

### 3.3.13 Voltage middle angle measurement enable control register: EnUAngle (Addrress: 0x2E)

Only when EnUAngle = 0x003584, ATT7022B can measure voltage middle angle. When EnUAngle ≠ 0x003584, ATT7022B can not measure voltage middle angle, scilicet voltage middle angle measurement function is disabled.

Note: It is recommended that we should open this function only when we need to output the middle angle values, otherwise we should close this function.

### 3.3.14 Current phase sequence detecting enable control register: EnDtIorder (Address: 0x30)

Only when EnDtIorder = 0x005678, ATT7022B can open current phase sequence detecting function. When EnDtIorder ≠ 0x005678, ATT7022B can not detect current phase sequence.

Note: It is recommended that we should open this function only when we need to output the current phase sequence values, otherwise we should close this function.

### 3.3.15 Voltage channel ADC gain select register: UADCPga (Address: 0x3F)

ATT7022B provides voltage channel ADC gain select register UADCPga, which is used to control amplificatory multiple of voltage channel ADC. In rated voltage Un, it is recommended that (the sampling signal Vu) * (amplificatory multiple) should be about 0.5v.

| Value of UADCPga | voltage channel ADC gain |
|---|---|
| 0x465500 | 2 |
| 0x465501 | 4 |
| 0x465502 | 8 |
| 0x465503 | 16 |
| 0xA5xxxx | Forbid be written |
| Other value | 1 |

### 3.3.16 Pulse constant reduplication select register: HFDouble (Address: 0x3E)

ATT7022B provides pulse constant reduplication select register: HFDouble, which is used to control pulse constant reduplication in small current mode. Scilicet in small current mode, we can magnify pulse constant via HFDouble register to speed up calibration.

Note: since this function is implemented by magnifying the value of power, only in small current mode we should use it. If we use this function on large signal, the power register will overflow and lead an unknown mistake.

| Value of HFDouble | Pulse constant reduplication rate |
|---|---|
| 0x5533CC | 2 |
| 0x5533CD | 4 |
| 0x5533CE | 8 |
| 0x5533CF | 16 |
| Other value | 1 |

### 3.3.17 Fundamental wave measurement enable control register: EnLineFreq (Address: 0x2D)

ATT7022B can provide fundamental wave and harmonic active and reactive energy pulse output directly, also provide apparent energy pulse output directly, which include RMS apparent energy and PQS apparent energy. These functions can be setup via EnLineFreq and EnHarmonic.

| Value of EnLineFreq | Value of EnHarmonic | Function |
|---|---|---|
| 0x007812 | ≠ 0x0055AA | Fundamental wave meter |
| | 0x0055AA | Harmonic meter |
| 0x008127 | ------ | RMS apparent energy meter |
| 0x005523 | ------ | PQS apparent energy meter |

| | | |
|---|---|---|
| Other value | ------ | Forbid above function |

### 3.3.18 Fundamental wave voltage power output select register: SelectPQSU (Address: 0x2F)

Fundamental wave active power, Fundamental wave reactive power, Fundamental wave apparent power, Fundamental wave phase angle, Fundamental wave power factor, and fundamental wave voltage parameter can be selected via SelectPQSU register. When SelectPQSU = 0x001228, corresponding power, voltage, phase, phase angle register would output fundamental wave parameter. When SelectPQSU ≠ 0x001228, corresponding power, voltage, phase, phase angle register would retain primary function.

### 3.3.19 Fundamental wave power calibration register: LineFreqPg (Address: 0x31)

ATT7022B provides Fundamental wave power calibration register: LineFreqPg, which can calibrate fundamental wave energy and apparent energy.

Fundamental wave power gain is calibration in power factor cos(Φ)=1. LineFreqPg should be cleared to zero before calibrate fundamental wave power, afterward we can calibrate fundamental wave power according to analogous method to section 3.4.4.

As known:

The error from standard meter: err

Formula:

LineFreqPg= $\frac{-err}{1+err}$

If LineFreqPg >= 0, then LineFreqPg = INT[LineFreqPg *$2^{23}$]

Else if LineFreqPg < 0, then LineFreqPg = INT[$2^{24}$+ LineFreqPg *$2^{23}$]

### 3.3.20 Fundamental wave measurement and harmonic measurement switched select register: EnHarmonic (Address: 0x3C)

As referred to section 3.3.19, harmonic meter mode is selected when register EnLineFreq = 0x007812 and EnHarmonic = 0x0055AA, here CF3/CF4 output harmonic pulse. Corresponding fundamental wave parameter is switched to harmonic parameter, including fundamental wave energy register switched to harmonic energy register, fundamental wave power and fundamental wave voltage switched to harmonic power and harmonic voltage.

## §3.4 Calibration flow chart and parameter calculation

### 3.4.1 Calibration flow

The standard energy meter is necessary to calibrate energy meters which are designed using ATT7022B. CF1 could be connected to the standard meter, then the calibrating could be done according to the error reading in standard meter. ATT7022B only need to calibrate active power, the reactive power need not to be calibrated. The calibration of fundamental wave meter and apparent meter please refer to the latter specifications.

**Calibration Flow Chart:**

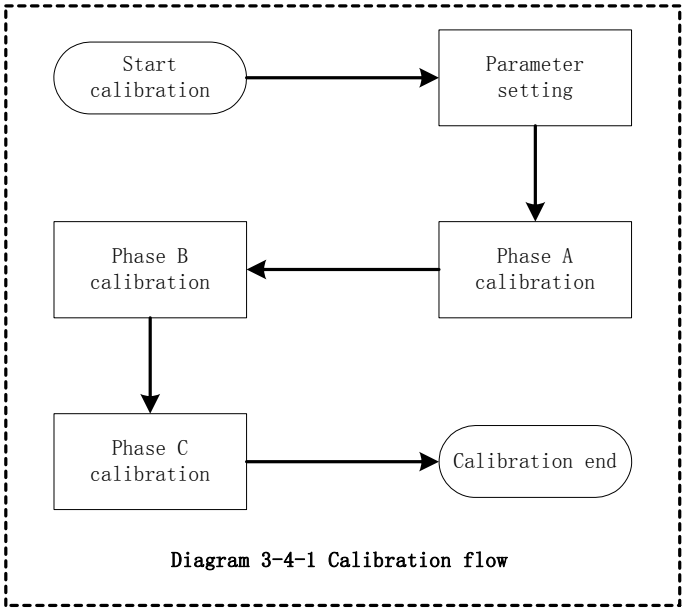



Diagram 3-4-1 Calibration flow

**Parameter setting:**

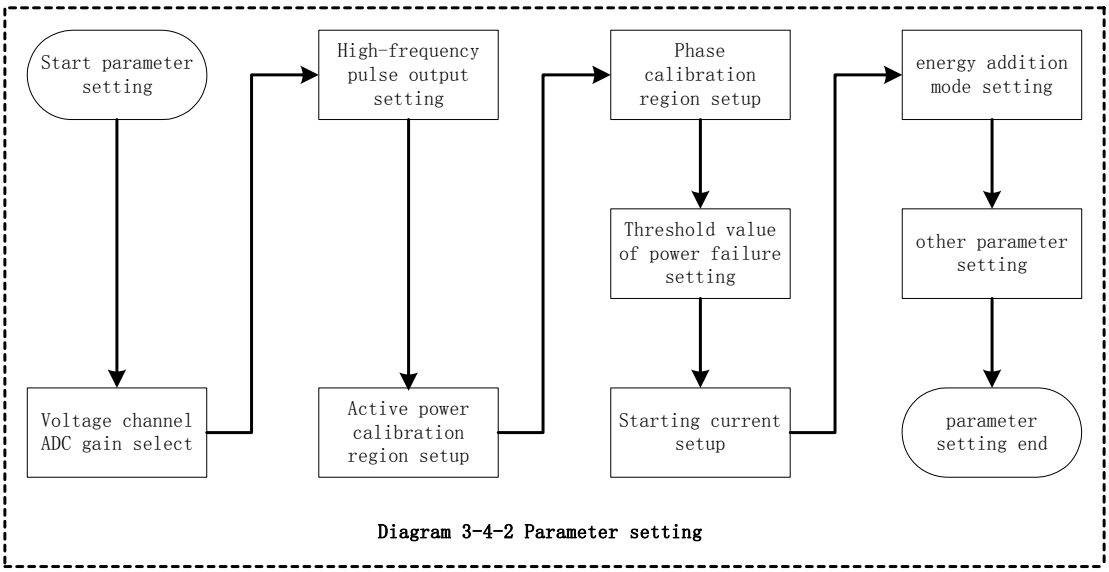



Diagram 3-4-2 Parameter setting

**Detached phase calibration:**

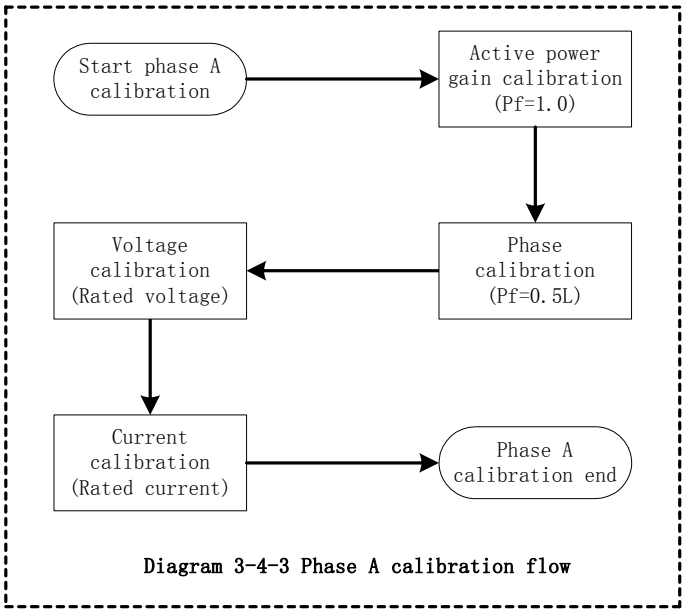



Diagram 3-4-3 Phase A calibration flow

In detached phase calibration, the calibration of detached phase current maybe influence the accuracy of A/B/C 3 phase current vector summation register IRmst. The current RMS calibration is described in the specification of current calibration register in section 3.3.8.

### 3.4.2 Fundamental wave/harmonic calibration

The fundamental wave and harmonic meter usually only need to be enabled after the calibration process according to section 3.4.1, needn't to be calibrated separately.

If we want to calibrate fundamental wave and harmonic, we must use fundamental wave/harmonic standard energy meter. The CF3 should be connected to the fundamental wave/harmonic standard meter, and the calibrating is according to the error reading in standard meter. Only the fundamental wave active power need to be calibrated, and the fundamental wave reactive power need not to be calibrated.

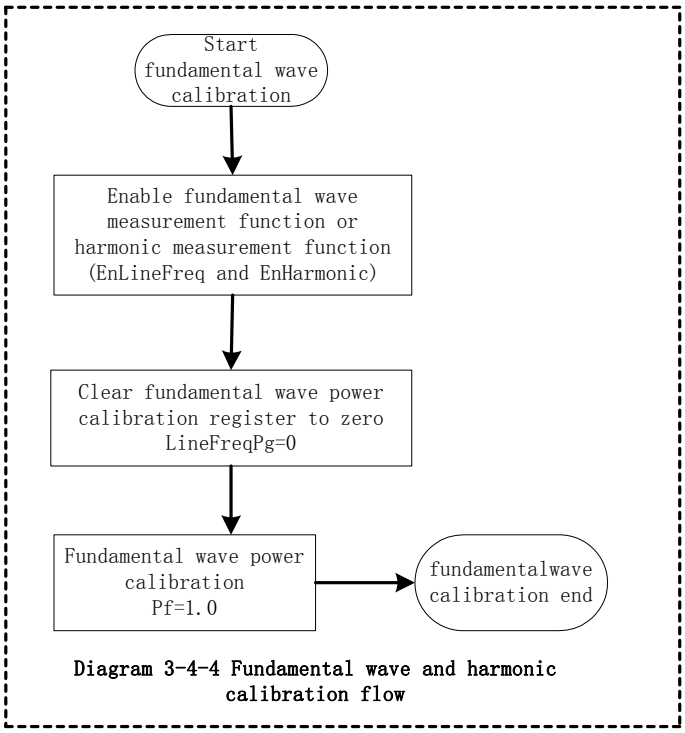



**Diagram 3-4-4 Fundamental wave and harmonic calibration flow**

### 3.4.3 RMS apparent energy calibration

RMS apparent energy measurement function usually only need to be enabled after calibration according to section 3.4.1, and the RMS apparent energy usually needn't to be calibrated.

If we want to calibrate RMS apparent energy, we must according to nether method. ATT7022B RMS apparent energy output via the CF3 port. The CF3 port should be connected to the apparent standard energy meter, and the calibrating should according to the error reading in standard meter.

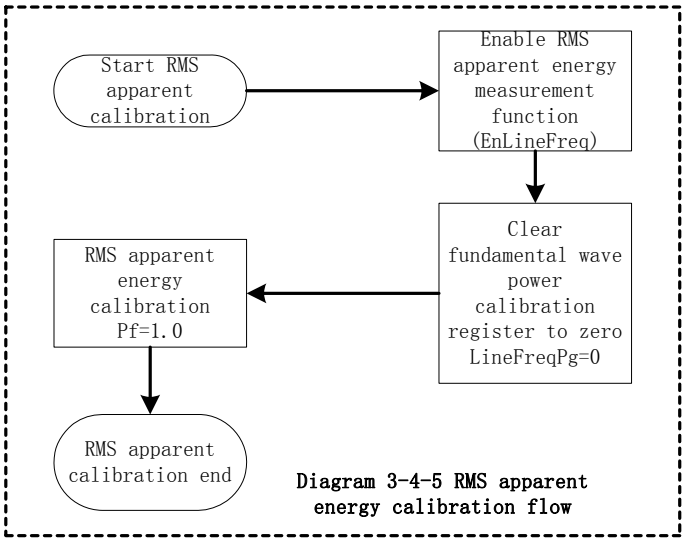



**Diagram 3-4-5 RMS apparent energy calibration flow**

### 3.4.4 PQS apparent energy calibration

PQS apparent energy measurement function usually only need to be enabled after calibration according to section 3.4.1, PQS apparent energy usually needn't to be calibrated.

If we want to calibrate PQS apparent energy, we must according to nether method. ATT7022B PQS apparent energy output via CF4 port. CF4 should be connected to the apparent standard energy meter, and the calibrating should according to the error reading in standard meter.

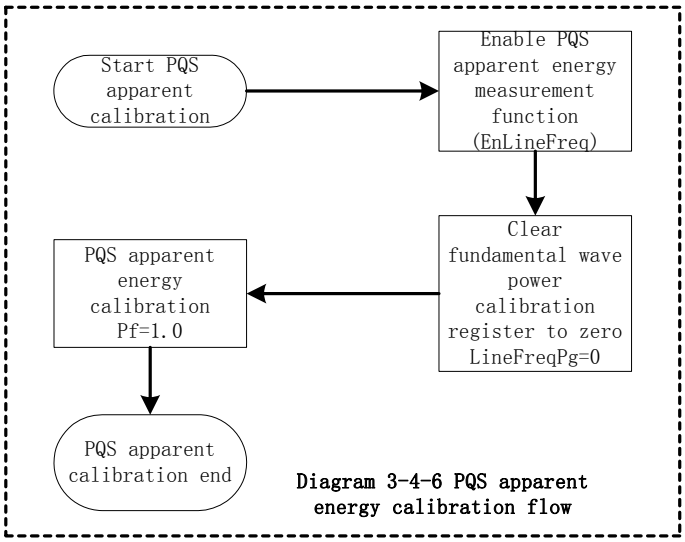



Diagram 3-4-6 PQS apparent energy calibration flow

# Chapter 4 SPI communication interface

## §4.1 SPI communication interface introduction

ATT7022B has a built-in SPI serial communication interface, which use passive working mode. The SPI have 2 control line and 2 data line: CS, SCLK, DIN, and DOUT.

CS: SPI selection signal (input pin), the control line of allowing accessing SPI. CS switches from high level to low level denotes SPI communication starting, CS switches from low level to high level denotes SPI communication ending. So when we start SPI communication, CS pin must be written a falling edge '↓'; when we stop SPI communication, CS pin must be written a rising edge '↑'.

DIN: serial data input (input pin), used to transmit data to ATT7022B.

DOUT: serial data output (output pin), used to read data from ATT7022B.

SCLK: serial clock (input pin), control data transmission rate. In SCLK falling edge '↓', the data on DIN pin is sampled to ATT7022B, In SCLK rising edge '↑', the data in ATT7022B is output to DOUT pin.

SPI communication interface is connected to external MCU as nether sketch map:

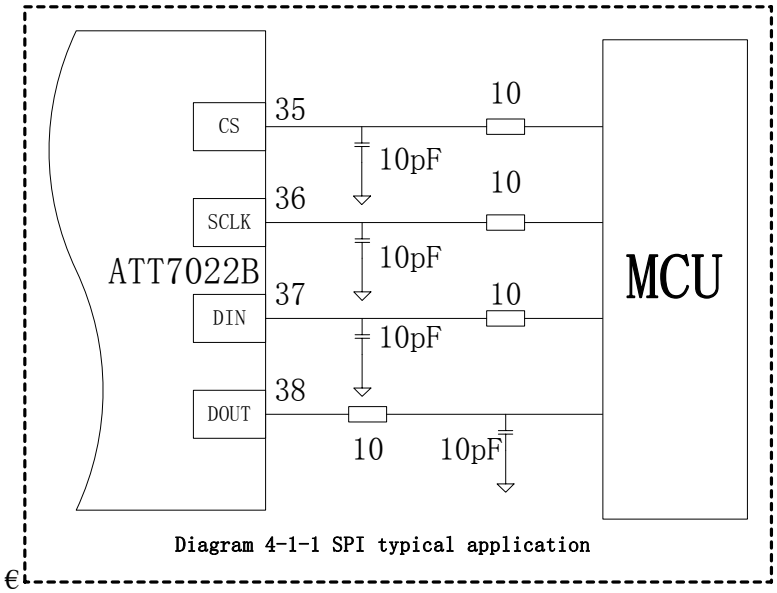



Diagram 4-1-1 SPI typical application

SPI signal line should be series connected a small resistance to prevent possible disturbance. This resistance associated with autoeciousness capacitance in chip's input port can compose a low pass filter, which could eliminate surge in SPI interface. It is recommended that a 10-100Ω resistance is used. If the autoeciousness capacitance in chip's input port is not big enough, we could use an external capacitance (about 10pF) at the input port. To select appropriate resistance and capacitance parameter, we should process some relevant experiments and analyze according to SPI transmission rate and the type of MCU.

## §4.2 SPI reading

All the measurement parameters and calibration parameters are transferred to external MCU via SPI.

**SPI reading timing:**

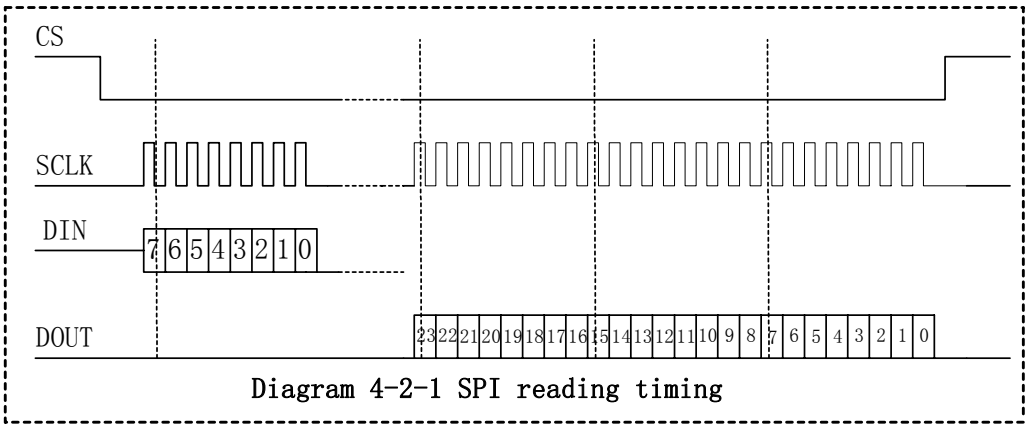



Diagram 4-2-1 SPI reading timing

**Command format meaning:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

Bit7=0: host MCU read measurement and calibration register from ATT7022B.

Bit7=1: host MCU write measurement and calibration data to ATT7022B.

Bit6...0: register address, refer to register definition section.

**SPI reading working procedure:**

After host MCU writes 8-bits command byte, a waiting period of time maybe needed, and then host MCU could read 24-bits data via SPI. Host MCU needn't wait if SCLK is less than 200 KHz. The waiting period of time is about 3us if SCLK is greater than 200KHz. Please refer to parameter output register specification section about data formats.

**Note:**

When transferring, the MSB is transmitted firstly and the LSB is transmitted lastly.

When SCLK is at high level, data on DIN or DOUT pin is updated. At every register's reading or writing the CS should be processed once.

**SPI reading demonstration:**

```
---------------------------------------------------------------------
01| ReadSpi(Byte Com)                    SPI
02| {                                    08|     for(n=7;n>=0;n--)
03|     ; Enable SPI                     09|     {
04|     CS=1;                            10|         SCLK=1;
05|     SCLK=0;                          11|         DIN=Com.n;
06|     CS=0;                            12|         SCLK=0;
07|     ; Send 8-bits Command to         13|     }
```

```
14|      ; waiting 3us
15|      delay(3);
16|      ; Read 24-bits Data From SPI
17|      for(n=23,Data=0;n>=0;n--)
18|      {
19|          SCLK=1;
20|          Data.n=DOUT;
21|          SCLK=0;
22|      }
23|      ; Disable SPI
24|      CS=1;
25|      ; Return Data From SPI
26|      return(Data);
27| }
28|
```

## §4.3 SPI writing

Host MCU can write calibration register in ATT7022B via SPI.

**SPI writing timing:**

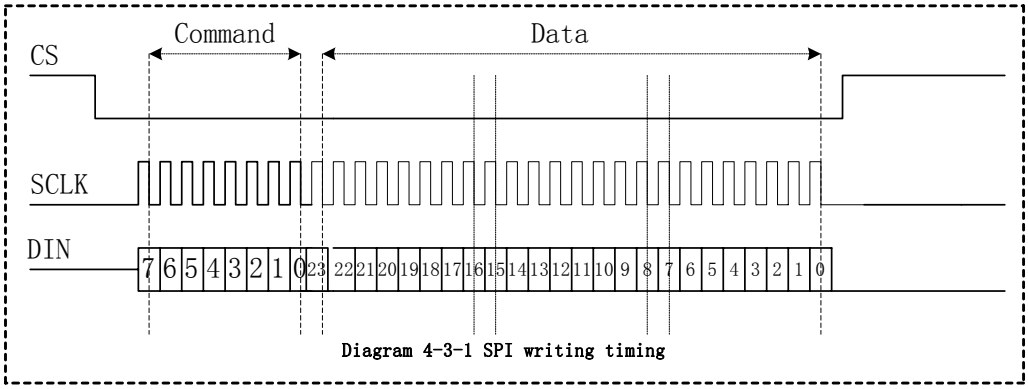



Diagram 4-3-1 SPI writing timing

**Command format meaning:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

Bit7/6 = 1 0: write command, used to update calibration data register.

Bit7/6 = 1 1: write special command; refer to write special command section.

Bit7 = 0: host MCU read measurement and calibration register from ATT7022B.

Bit5...0: register address, refer to register definition section.

**SPI writing working procedure:**

After host MCU write 8-bits command byte, host MCU needn't wait and can write 24-bits data via SPI immediately.

**Note:**

When transferring, the MSB is transmitted firstly, the LSB is transmitted lastly.

**SPI writing demonstration:**

---

```
01| WriteSpi(Byte Com,UINT Data)
02| {
03|      ; Enable SPI
04|      CS=1;
05|      SCLK=0;
06|      CS=0;
07|      ; Send 8-bits Command to SPI
```

```
08|     for(n=7;n>=0;n--)
09|     {
10|         SCLK=1;
11|         DIN=Com.n;
12|         SCLK=0;
13|     }
14|     ; Send 24-bits Data to SPI
15|     for(n=23,Data=0;n>=0;n--)
16|     {
17|         SCLK=1;
18|         DIN=Data.n;
19|         SCLK=0;
20|     }
21|     ; Disable SPI
22|     CS=1;
23| }
24|
```

---

## §4.4 SPI write special command

ATT7022B provides special command to cooperate with software calibration and the operation process is consistent with SPI writing operation timing.

**SPI write special command timing:**

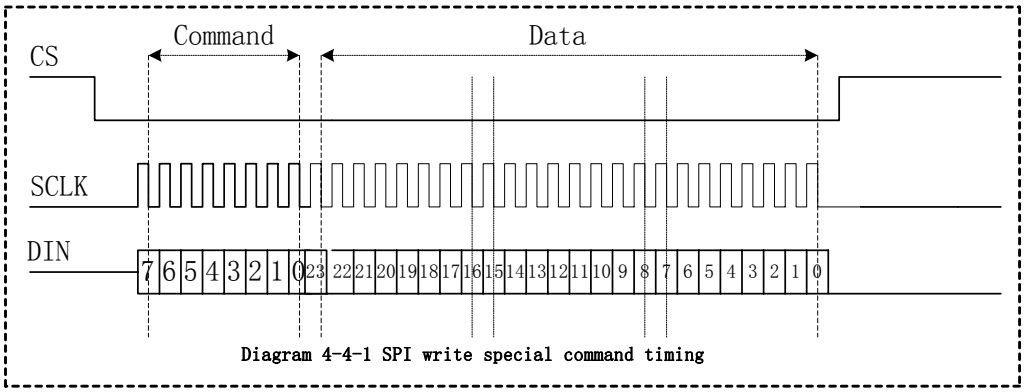



Diagram 4-4-1 SPI write special command timing

**Command format meaning:**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

Bit7/6 = 1 1: write special command.

Bit7/6 = 1 0: write command, used to update calibration data register.

Bit7/6 = 0 X: read command, host MCU read measurement and calibration register from ATT7022B.

Bit5...0: the type of special command.

**SPI write special command working procedure:**

After host MCU write 8-bits command byte, host MCU needn't wait and can write 24-bits data via SPI immediately.

**Noticed:**

When transfer, the MSB is transmitted firstly, the LSB is transmitted lastly.

**Special command specification:**

ATT7022B special command includes: 0xC3, 0xC6, 0xC9, and 0xD3.

| Special command | 8-bits command | 24-bits data | Special command specification |
|---|---|---|---|
| Clear calibration data | 0xC3 | 000000 h | Sending 0xC3000000 can resume calibration data register to reset initialization. |
| Read calibration data | 0xC6 | 00005A h | Sending command=0xC6 and data≠ 0x00005A can read data register (00-7FH) via SPI.<br>Sending command=0xC6 and data= 0x00005A can read calibration data register via SPI, and can not read 00-7FH register.<br>When reading calibration data register, the reading value from 0x00 is 0xAAAAAA invariable, or else ≠ 0xAAAAAA. |
| Enable writing calibration data | 0xC9 | 000000 h or 000001 h | Sending 0xC9000000 can enable SPI calibration data writing operation, here host MCU could modify calibration data register via SPI. Host MCU can read the last written data from 0x002D/0x002E register after enabling SPI writing operation.<br><br>Sending 0xC9000001 can disable SPI calibration data writing operation, that could prevent calibration data register from being written in error. After SPI calibration data writing operation is closed, if host MCU writ SPI port, the read data from 0x002D/0x002E is 0x200361 invariable. |
| Software reset | 0xD3 | 000000 h | Sending 0xD3000000 can reset ATT7022B. |

# Chapter 5 Electrical Characteristics

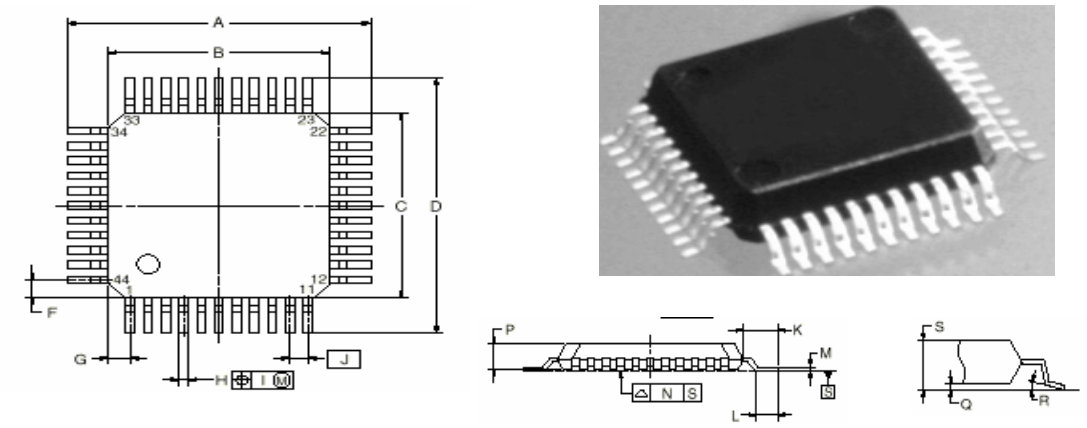
## §5.1 Electrical parameter

| Test object | minimum | typical | Max | unit | Test condition |
|---|---|---|---|---|---|
| VCC | 4.75 | 5 | 5.25 | V | |
| VDD | | 3.0 | | V | |
| Reference voltage | 2.3 | 2.4 | 2.6 | V | |
| Reference power TC | | 30 | | ppm | |
| Input voltage range | | | ±1.5 | V | Difference input Vpp |
| VOH(CF1,CF2, CF3, CF4,REVP) | 4.5 | | | V | IOH=5mA |
| VOL(CF1,CF2, CF3, CF4,REVP) | | | 0.5 | V | IOL=5mA |
| Logic input high-level[1] | 2.5 | | | Vmin | |
| Logic input low-level[1] | | | 0.8 | Vmax | |
| Logic output high-level[2] | 2.5 | | | Vmin | Ioh=2mA |
| Logic output low-level[2] | | | 0.8 | Vmax | Iol=2mA |
| Reference voltage output resistance:<br>Minimum load resistance<br>Maximum load capacitance | <br>2 | 130 | <br><br>100 | Ω<br>KΩ<br>pF | |
| Positive power supply current | | 28 | | mA | VDD=3.0V ; VCC=5V |
| ADC bit digit | | 16 | | bit | |
| ADC sampling speed | | 3.2 | | kHz | |
| ADC dynamic range | | 88 | | DB | |
| ADC whole harmonic distortion | | -95 | | DB | |
| ADC channel disturbance | | -92 | | DB | |
| Crystal frequency | | 24.576 | | MHz | |
| Temperature range | -40 | | 85 | ℃ | |

Note 1: denotes CS, SCLK, DIN, SEL.
Note 2: denotes DOUT.

## §5.2 Packaging information

Packaging information: 44Pin QFP (Quad Flat Package 10X10 )




**NOTE**1.Controlling dimension ---millimeter.

2.Each lead centerline is located within 0.12mm(0.005inch) of its true position (T.P.)at maximum material condition

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 13.6±0.4 | 0.535 $^{+0.017}_{-0.016}$ |
| B | 10.0±0.2 | 0.394 $^{+0.008}_{-0.009}$ |
| C | 10.0±0.2 | 0.394 $^{+0.008}_{-0.009}$ |
| D | 13.6±0.4 | 0.535 $^{+0.017}_{-0.016}$ |
| F | 1.0 | 0.039 |
| G | 1.0 | 0.039 |
| H | 0.35 $^{+0.08}_{-0.07}$ | 0.014±0.003 |
| I | 0.15 | 0.006 |
| J | 0.8 (T.P.) | 0.031 (T.P.) |
| K | 1.8±0.2 | 0.071 $^{+0.008}_{-0.009}$ |
| L | 0.8±0.2 | 0.031 $^{+0.009}_{-0.008}$ |
| M | 0.17 $^{+0.08}_{-0.07}$ | 0.007 $^{+0.003}_{-0.004}$ |
| N | 0.10 | 0.004 |
| P | 2.7±0.1 | 0.106 $^{+0.005}_{-0.004}$ |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 3° $^{+7°}_{-3°}$ | 3° $^{+7°}_{-3°}$ |
| S | 3.0 MAX | 0.019 MAX |

| | |
|---|---|
| NEC CODE | P44GB-80-3B4-4 |
| EIAJ CODE | |
| Weight(Reference Value) | 0.54g |